+ &) $

$ 5 0 Š & R U Š W H [

HC32F4A0LRQIFTPB100 / HC32L2QHF4PA100R0GTB

HC32F4A0LRQIFTPB144 / HC32L2QFF4PA104R4GTB

HC32F4A0LSQIFTPB176 HC32F4A0QSFCTB176

HC32F4A0VSFIBHGBA176 HC32F4A0FSBCGHAB176

HC32F4A0TTFIBHGBA208

ARM Cortex-M4 32bit MCU 240MHz 256KB Flash 96KB SRAM USB FS/HS OTG Ethernet MAC 2 CAN FD/2.0B 4 I2S QSPI AES HASH HA25MAC FMAC FIR MAU 4 PGA 4 CMP 16 UART 6 SPI 6 I2C 4 I2S QSPI AES HASH HA25MAC FMAC FIR MAU

- ARM-M4 32bit Cortex-M4 CPU FPU MPU SIMD DSP ETM CoreSight 240MHz 300DMIPS 825 Coremark
- 256KByte 4KByte 2 Flash memory
- 96KByte SRAM 12KByte RAM
- Vcc 1.8~3.6V
- 6 4~25MHz 32.768kHz 8 RC16/20MHz RC8MHz RC32kHz WDT RC 128Hz
- POR (PVD1R/PVD2R) NRST 15
- Sleep Stop Standby power down
- VBAT RTC 128Byte 4KByte SRAM
- 16 DMAC
- USBHS USBFS 8 DCU
- MAU Sin/Sqrt
- 16 FIR FMAC
- AOS
- 3 12bit 5MSPS ADC
- 3
- 4 12bit 15MSPS DAC
- 4 PGA
- 4 CMP
- 1 OTS
- 8 32/16bit PWM Timer 16 250ps PWM HRPWM
- 3 16bit PWM Timer
- 12 16bit TimerA
- 4 16bit Timer
- 2 16bit Timer
- TimerRTC
- 2 WDT
- 142 GPIO 134 5V-tolerant IO 32
- 10 USART ISO7816-3
- 6 SPI
- 6 I2C SMBus
- 4 I2S PLL
- 2 SDIO SD/MMC/eMMC
- 1 QSPI 24Mbps XIP
- 2 CAN CAN2.0B, CAN FD
- 2 USB 2.0 HS FS FS PHY Device Host
- 1 10/100 EMAC IEEE-1588 MII RMII EXMC
- Memory
- Memory
- AES/HASH HA25MAC/TRNG

LQFP176 24×24mm LQFP144 20×20mm LQFP100 14×14mm WFBGA117 6×10mm TFBGA216 13×13mm

“XHSC”

/ XHSC

XHSC

XHSC

XHSC XHSC

“ ® ” “ ™” XHSC XHSC

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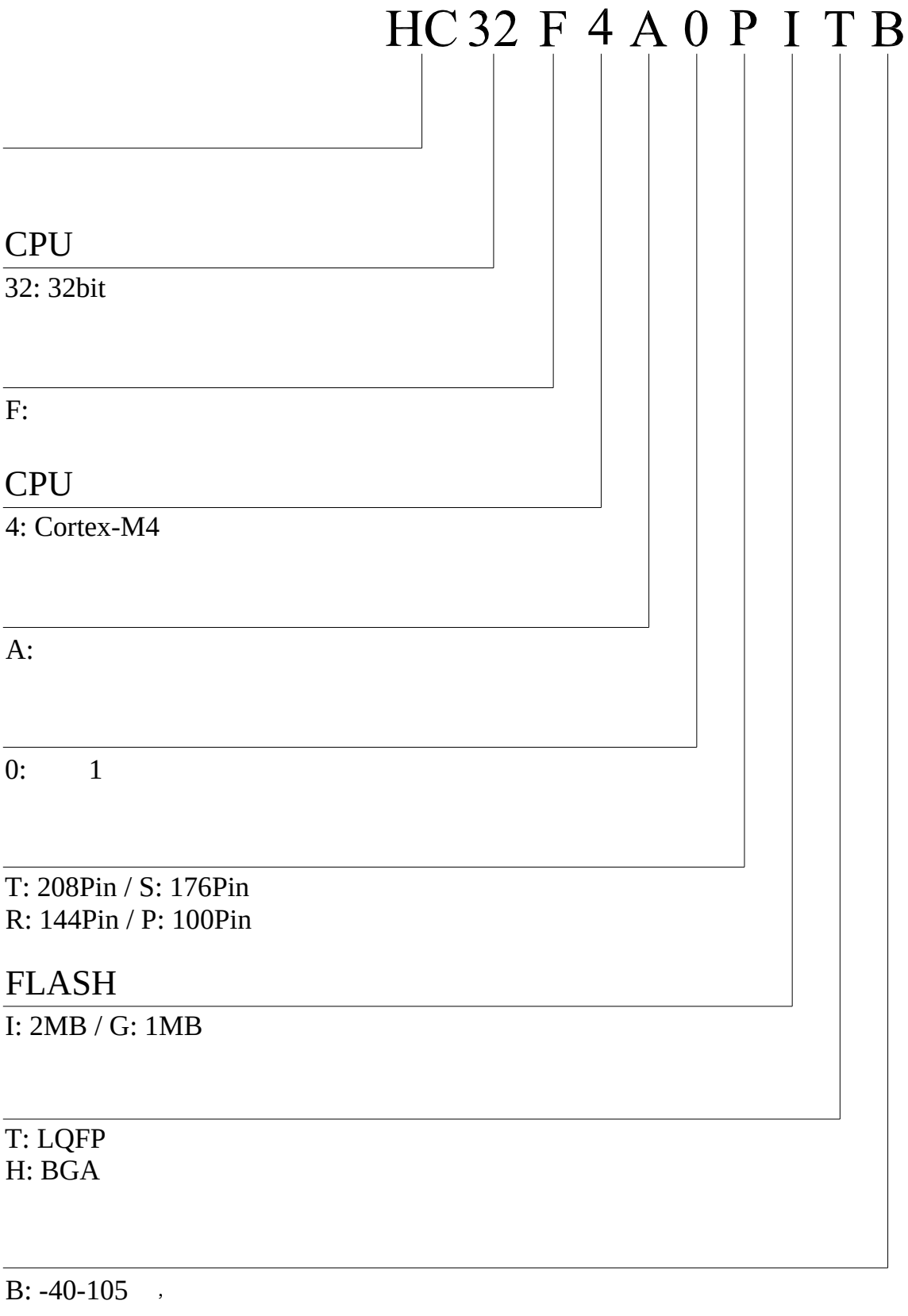
3．3．7．2 MRC 82
3．3．7．3 LRC 82
3．3 SWDT SWDTLRC 83
3．3 RTC RTCRC 83
3．3．8 PLL 84
3．3．9 85
3．3．10 86
3．3．10．1 ESD 86
3．3．10 Layout 86
3．3．11 I/O 87
3．3．12 PWM 91
3．3．13 I2C 92
3．3．14 SPI 93
3．3．15 QSPI 96
3．3．16 I2S 98
3．3．17 CAN FD/ CAN2．0B 100
3．3．18 USB 100
3．3．19 ETHMAC 103
3．3．19．1 103
3．3．19．2 MII 104
3．3．19．3 RMII 105
3．3．20 UART 106
3．3．21 JTAG 107
3．3．22 SWD 109
3．3．23 TM 110
3．3．24 12 ADC 111
3．3．25 12 DAC 118
3．3．26 121
3．3．27 121
3．3．28 XMC 122
3．3．29 VP 124
3．3．30 SD/ SDIO MMC Card host interface (SDIO) 125
3．3．31 129
3．3．32 VBAT 130
3．3．33 IRQ 130
3．3．34 USART1 STORX 131
3．3．35 USB PHY STOP 131
4 132
4．1 132
4．2 137
4．3 142
4．4 143

5 144
& 145

3-39 127
3-40 127

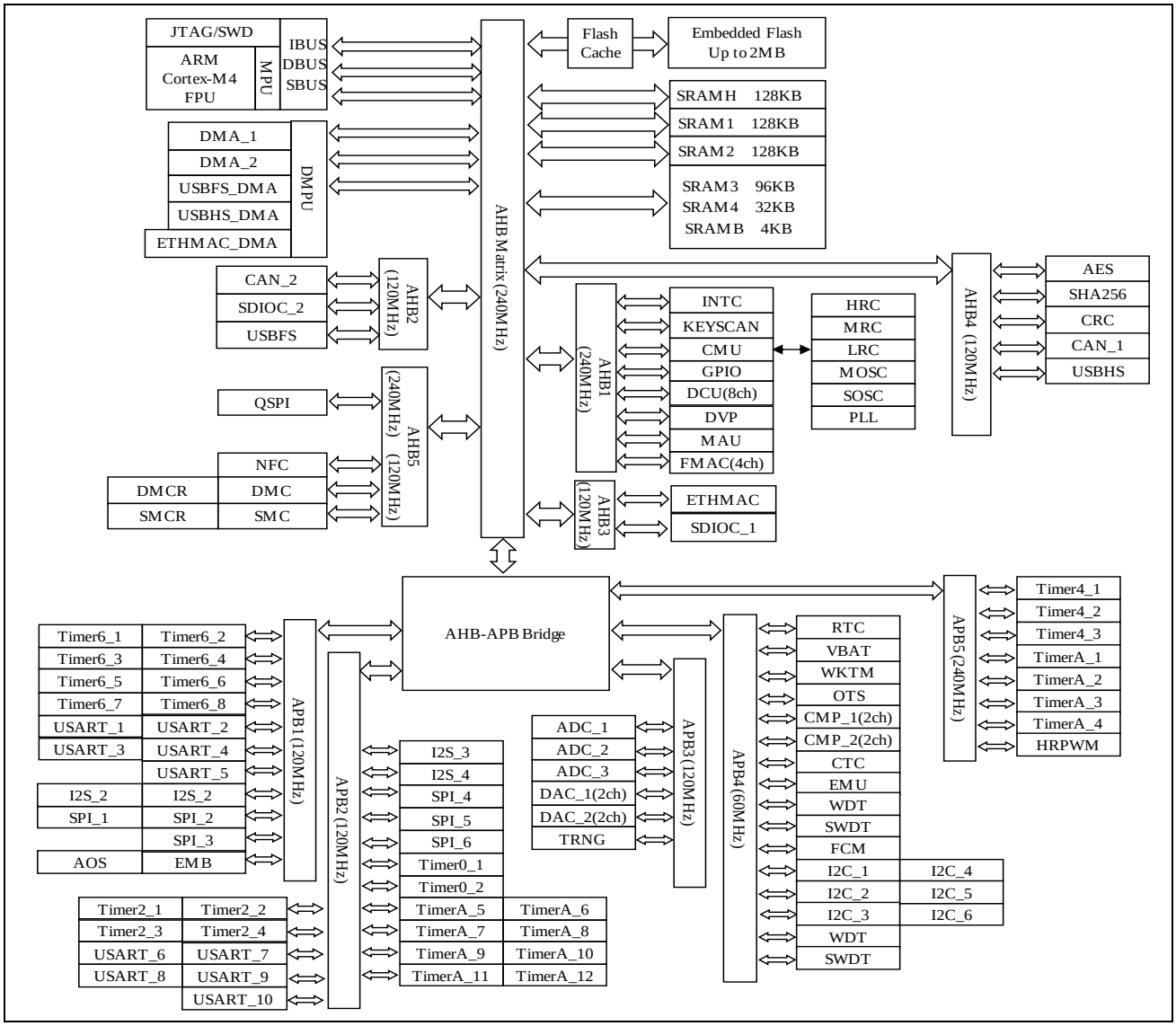
1.1


HC 32 F 4 A 0 P I T B
CPU
32: 32bit
F:
CPU
4: Cortex-M4
A:
0: 1
T: 208Pin / S: 176Pin
R: 144Pin / P: 100Pin
FLASH
I: 2MB / G: 1MB
T: LQFP
H: BGA
B: -40-105 ,

DVP	√
DCU	√
FMAC	√
MAU	√
AES256	√
HASHSHA256	√
TRNG	√
EXMC	√
FCM	√
(PVD	√
	SWD
	JTAG

1-1

1.3


JTAG/SWD
ARM Cortex-M4 FPU
MPU
IBUS
DBUS
SBUS
Flash Cache
Embedded Flash Up to 2MB
SRAMH 128KB
SRAM1 128KB
SRAM2 128KB
SRAM3 96KB
SRAM4 32KB
SRAMB 4KB
DMA_1
DMA_2
USBFS_DMA
USBHS_DMA
ETHMAC_DMA
DMPU
AHB Matrix (240MHz)
CAN_2
SDIOC_2
USBFS
AHB2 (120MHz)
QSPI
NFC
DMCR
DMC
SMCR
SMC
AHB5 (240MHz) (120MHz)
AHB1 (240MHz)
INTC
KEYSCAN
CMU
GPIO
DCU(8ch)
DVP
MAU
FMAC(4ch)
HRC
MRC
LRC
MOSC
SOSC
PLL
AHB4 (120MHz)
AES
SHA256
CRC
CAN_1
USBHS
AHB3 (120MHz)
ETHMAC
SDIOC_1
AHB-APB Bridge
APB1 (120MHz)
Timer6_1
Timer6_2
Timer6_3
Timer6_4
Timer6_5
Timer6_6
Timer6_7
Timer6_8
USART_1
USART_2
USART_3
USART_4
USART_5
I2S_2
I2S_2
SPI_1
SPI_2
SPI_3
AOS
EMB
APB2 (120MHz)
I2S_3
I2S_4
SPI_4
SPI_5
SPI_6
Timer0_1
Timer0_2
TimerA_5
TimerA_6
TimerA_7
TimerA_8
TimerA_9
TimerA_10
TimerA_11
TimerA_12
Timer2_1
Timer2_2
Timer2_3
Timer2_4
USART_6
USART_7
USART_8
USART_9
USART_10
APB3 (120MHz)
ADC_1
ADC_2
ADC_3
DAC_1(2ch)
DAC_2(2ch)
TRNG
APB4 (60MHz)
RTC
VBAT
WKTM
OTS
CMP_1(2ch)
CMP_2(2ch)
CTC
EMU
WDT
SWDT
FCM
I2C_1
I2C_2
I2C_3
WDT
SWDT
I2C_4
I2C_5
I2C_6
APB5 (240MHz)
Timer4_1
Timer4_2
Timer4_3
TimerA_1
TimerA_2
TimerA_3
TimerA_4
HRPWM

1-1

– APB5 (Timers/HRPWM)

– AHB1

(DMPU/KEYSCAN/INTC/DCU/GPIO/DMA/CMU/DVP/

– AHB2 (CASNDICODUSBFS)

– AHB3 (SDIOC/ETHMAC)

– AHB4 (AES/HASH/CRC/CAN/USBHS

– AHB5 (SMCDMSCMCR/DMNCFRCQ/SPI

1.4.3 508

15

POR

NRST NRST

BOR

1 PVD1R

2 PVD2R

WDTR

SWDTR

PDRST

SRST

MPU MPUR

RAM RAMPR

RAMECC RAMECCR

CKFER

XTALER

Cor-M4x LOCKUPLKUPR

1.4.4 &08

P L L

R T C S WD T

F C M

A H B A P B C o r - M 4 x 6

1 X T A L

2 X T A L 3 2

3 P L L H P L L H

4 H R C

5 MR C

6 L R C

2 4M0Hz S WD T S WD T

S WDIT R C R T C ~FO _9‘ ~

U S -F S 4 8 MHz , P L L H , P L L A

1.4.5 3 : &

PVD1 VCC PVD2

VCC

ADC VBAT

VBAT VBAT VBAT

1.8V 2.0V VBAT ADC VBAT 1/2

VBAT

VCC VBAT (RTC)

(WKTM) RLDO VDDR

VCC RLDO 4KB SRAM(Backup

SRAM)

1.4.6 ,&*

FLASH 0x0 000400 0~0x0 0400F0

0x0 000408 0x0 0408 0x0 000401 0~0x0 041F0 0 0

0x0 000208 00x0 0004 5F 1 FLASH

FLASH H0 0 FLASH

FLASH H1 0 0 (Initial Con

0x0 000200 0x0 0407 FLASH

1.4.7)/$6+ ()0

FLASH ICODE DCODE MCODE FLASH FLASH

FLASH dual bank BGO background operation

134Kbyte OTP

ICODE 16Bytes

ICODE 4Kbyte (256x128)DCODE

1Kbyte (64x128)8

1.4.8 65$0 65$0

4KB SRAMSRAMB 51K2B SRAM
SRAMH/ SRAM1/ SRAM24 SRAM3/ SRAM
SRAM 16 32 SRAMSRAMH
CPU 240MHz0 1
SRAM SRAM SRAM_WTCR

SRAMB Power down 4KB
SRAM4 SRAMB ECC Error CheckingECCd Correct
SRAMH/ SRAM1/ SRAM2/ SRA
Evepmarity check

1.4.9 ,2 *3,2

GPIO
Port16 I/O Pin 16

I/O pin I/O pi6m4
I/O pin
I/O pin 2 2

1.4.10 ,17&

INTC NVIC WFI
WFE

1.4.16 &03

Comparator CMP

CMP~4

CMP

CMP 1 ~ 4

CMP 2 CMP 4

PWM

VCOUT

1.4.17 $'&

12 ADC MCU 3 ADC

1 2 16 3 20

ADC

$'&

– 12 10 8

– ADC PCLK4 PCLK2 ADCLK
1：12：14：18：11：21：4
PCLK2 HCLK PLL
PCLK4：PCLK2 = 1：1
PCLK2 60 MHz
– 2.5 MSPS PCLK2 = 60 MHz 11 13
–
–
– /
–
–
– ADC

– 16
– 2 VBAT

–
–
–

– 2 A B
– A
– A
– A B B A
– ADC

– A ADC_EOCA
– B ADC_EOCB

– 0 ADC_CMP0

– 1 ADC_CMP1

– 4 DMA

MCU 4 PGA x2~x32

PGA ADC

MCU 3 SH

SH ADC

A/D

SH

1.4.18 '$&

MCU 12 - DAC1 DAC2 DAC

D/A

VREFHVREFL

'$&

DAC D/A

12

DAC

DCU

A/D A/D

VREFVHR/EFL

1.4.19 276

OTS

OTS

1.4.20 7LPHU

6 Timer 16

PWM

PWM PWM

PWM PWM PWM

2 3

EMB 8 Timer U1~4 32bit U5~U8

16bit

1.4.21 3:0 +53:0

PWMHRPWM Timer PWM TMR6

16 PWM

HRPWM

PWM

PWM

1.4.22 7LPHU

4 Timer

PWM EMB 3 Timer

1.4.23 (0%

PWM

P WM

1.4.24 7LPHU

A Ti mer 1 6 4 P WM

P WM P WM

P WM

3 2 2 3

1 2 Ti mer 4 8 P WM

1.4.25 7LPHU

2 Ti mer

2 CHA CHB

2

4 Ti mer

1.4.26 7LPHU

0 Ti mer

2 CHA CHB

2

Ti mer

1.4.27 57&

(RTC) BCD 00 99

12 / 24 2829

30 31

1.4.28 :'7

R C S WDI T R C 0 K 1 H z

S WD T P C L K 3 WD T

16

1.4.29 8 6 $ 5 7

U S A R T 1 0 U S A R T

U S A R T

U A R T (I S O / I E - 3) 7 8 L I 1 N 6

(C T S / R T S T i m e r 0 U A R T

T I ME O U T US A R T _ 1 RX ST O P

UA R T

RX ST O P US A R T _ 1

U S A R T _ U S 1 A R T _ U 2 A R T _ U 3 S A R T _ U S 4 A R T _ U 6 S A R T _ 7

US A R T _ U 8 S A R T _ 9

L I N U S A R T _ U 5 S A R T _ 1 0

U S A R T _ U S 1 A R T _ U 2 S A R T _ U 3 S A R T _ U S 4 A R T _ U 6 S A R T _ 7

US A R T _ U 8 S A R T _ 9

UA R T U S A R T _ U S 1 A R T _ U 2 S A R T _ U 6 S A R T _ 7

1.4.30 , &

I2C I2C

I2C SMBus

I2C :

1) I2C SMBUS

2) 10Kbps 400Kbps

3)

4) 2 7 10
SMBus SMBus SMBus

5)

6)

7)

8) SCL

9) SCL SDA

10)

1.4.31 6 3 ,

6 S P I

/ /

	1
	• 4 S P I 3 • • S C K
	• : MS B / L S B • : 4 / 5 / 6 / 7 / 8 / 9 / 1 0 / 1 1 / 1 2 • 4 3 2
	• P C L K 2 ~ 2 5 6 • P C L K 6
	• 1 6 •
	• • • •
	• • • •
	• •

	• • • SPI / / / • SPI •
	• SPI

1-2 SPI

1.4.32 463,

QSPI SPI

ROM EEPROM FeRAM

1.4.33 , 6

I2SInter_IC Sound Bus

	16/32 16/24/32 MSB

8

	4 32 FIFO
	I2SCLK(UPLLR/UPLLQ/UPLLP/MPLLR/MI2S_EXCK

CAN FD 1 Primary Tran
Buffer PTB 3 Secondary Transmit Bu
STB 8
Receive BuffRBr 3 STB 8 RB
3 FIFO 8 FIFOIFO
CAN FD CAN Timetrigger communi

1.4.37 &$1 % &$1 %

CAN2.0B CAN CAN2.0A(CAN2.0B
CAN CAN2.0B 16

CAN2.0B 1 Primary Tran
Buffer PTB 3 Secondary Transmit Bu
STB 8
Receive BuffRBr 3 STB 8 RB
3 FIFO 8 FIFOIFO
CAN2.0B CAN Timetrigger communi

1.4.38 6',2 6',2&

SDIOC SD MMC SD2.0 SD
SDIO e MMC4.2 MMC 2 SDIO
2 SD MMC/SDIO
SDIOC
SDSCSDHCSDXC SD SDIO
(1 b)it (4 b)SD
(1 b)it (4 b)it (8 b)MMC
SD 50MHz

1.4.39 0$& (7+0$&

MAC ETHMAC IEEE8-2002.3

MAC

PHY MII IEEE802.3

RMII

- IEEE8-2002.3 MAC
- IEEE1-2508088
- AMBA2.0 AHB /
- RMII

1.4.40 (;0&

EXMCExternal Memory Controller

EXMC AMBA

SRAMPSRAMNOR FlashNAND

Flash SDRAM EXMC

1.4.41

E T M

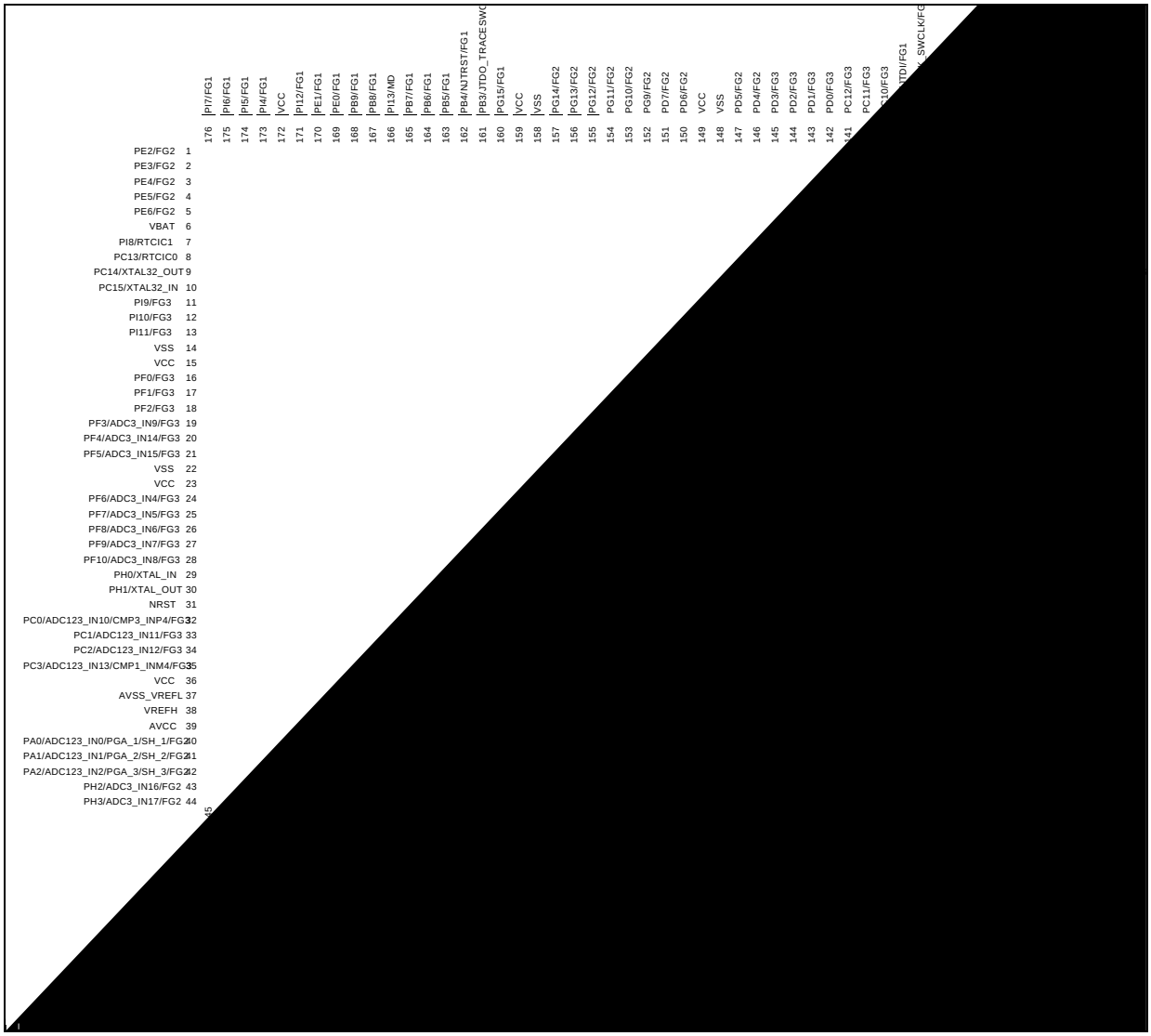
S WD

J T A G

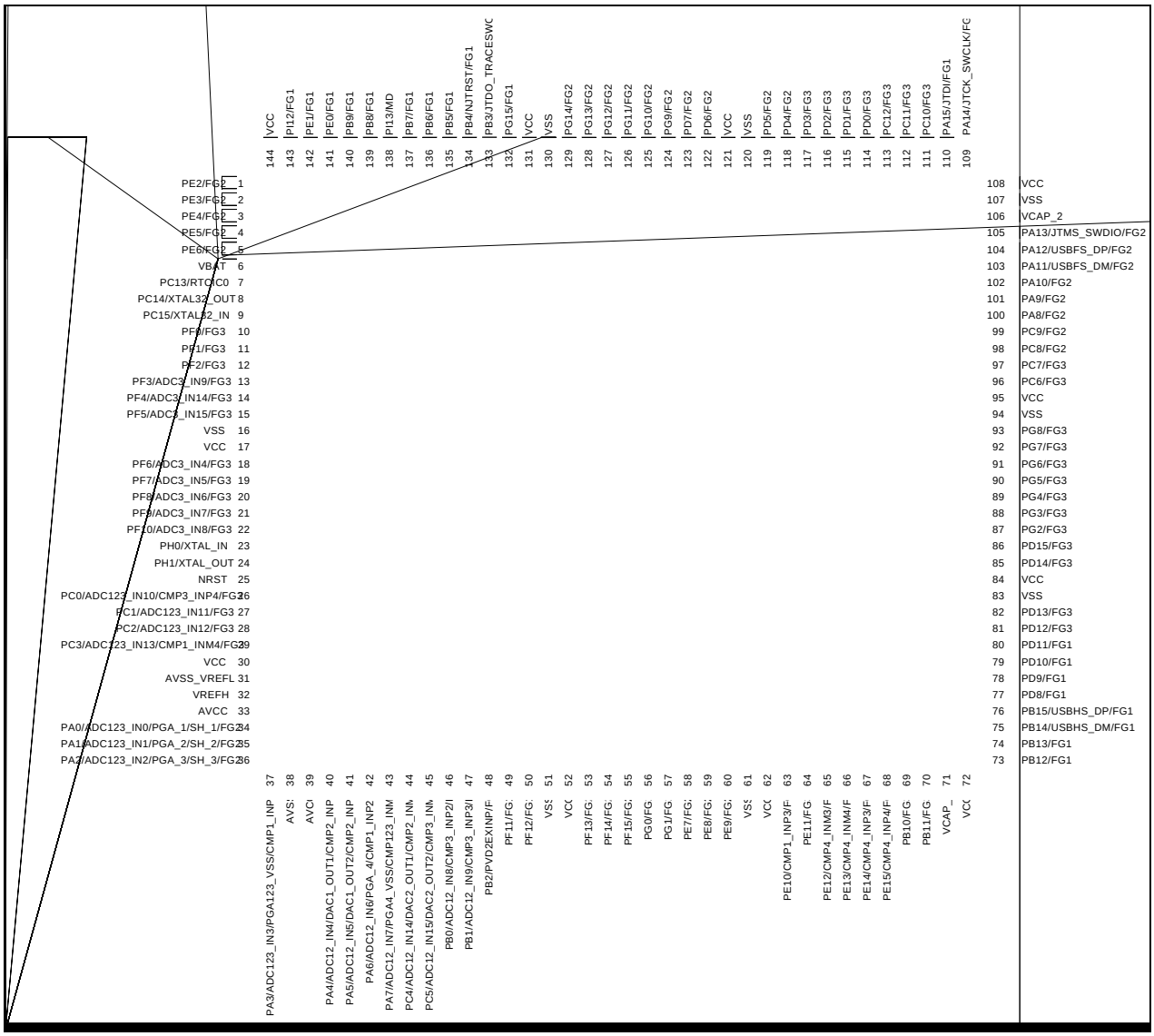
2 Pinouts

2.1

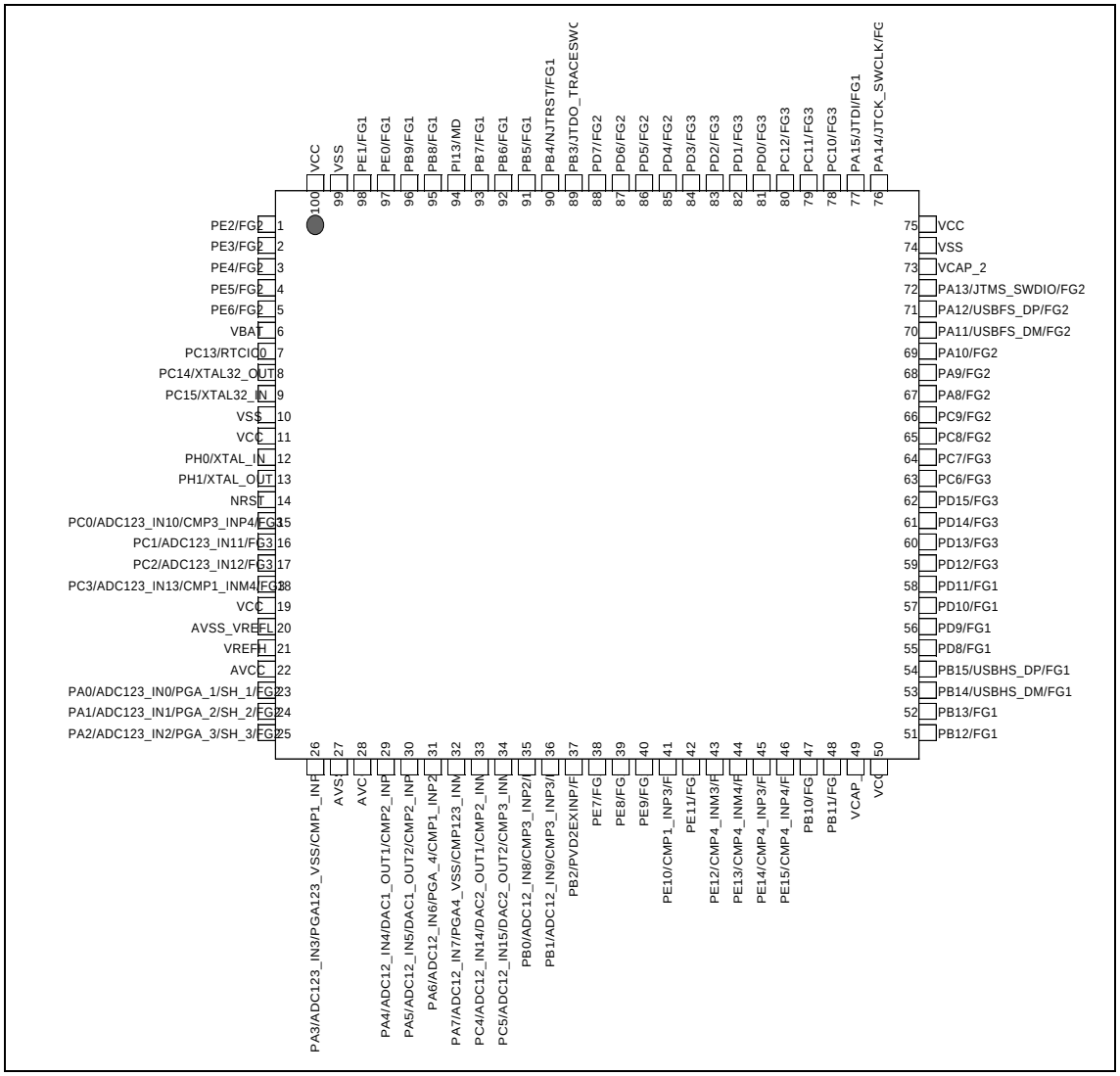
LQFP176



LQFP144

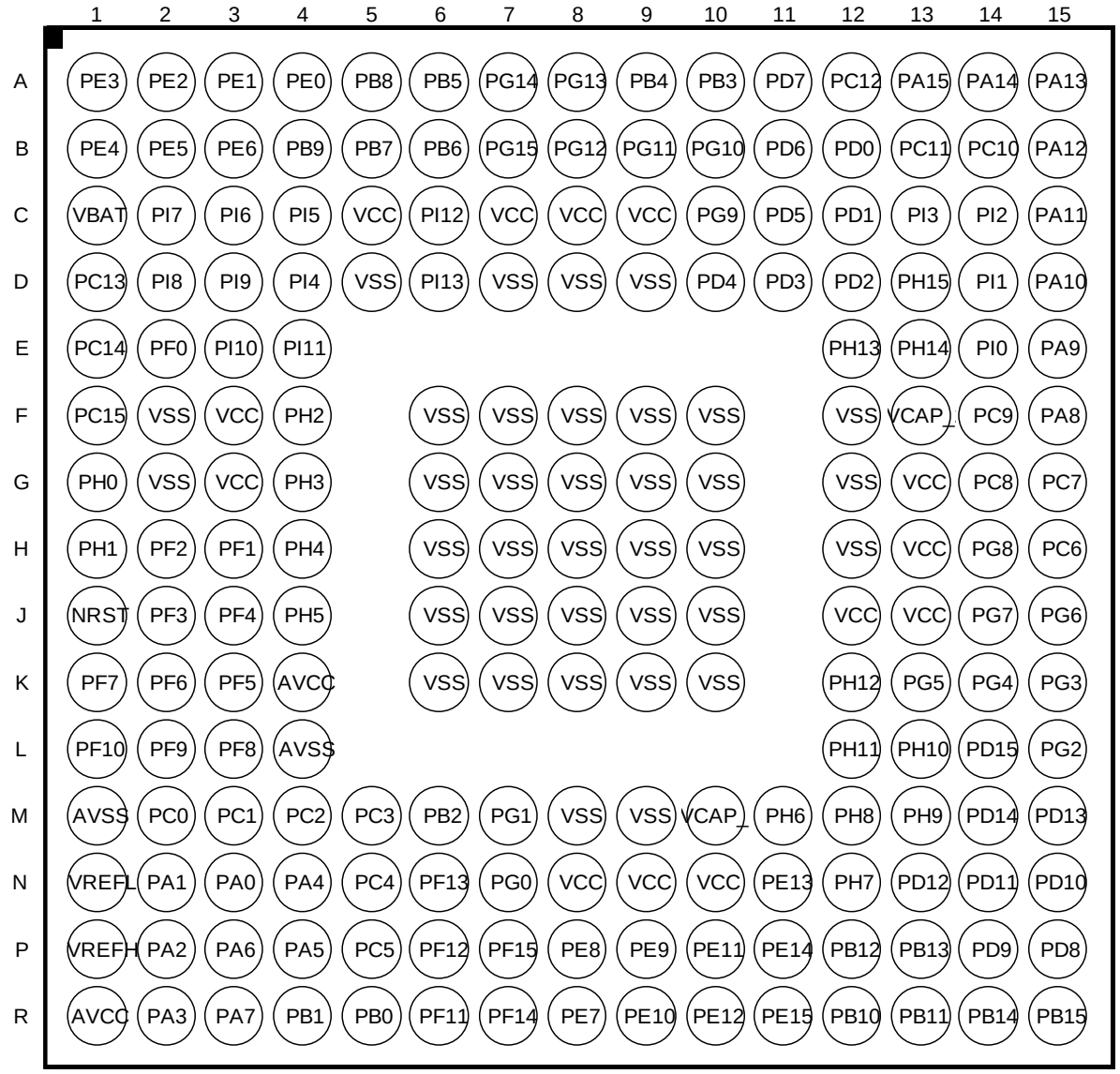

1 PE2/FG2
2 PE3/FG2
3 PE4/FG2
4 PE5/FG2
5 PE6/FG2
6 VBAT
7 PC13/RTCC0
8 PC14/XTAL32_OUT
9 PC15/XTAL32_IN
10 PF0/FG3
11 PF1/FG3
12 PF2/FG3
13 PF3/ADC3_IN9/FG3
14 PF4/ADC3_IN14/FG3
15 PF5/ADC3_IN15/FG3
16 VSS
17 VCC
18 PF6/ADC3_IN4/FG3
19 PF7/ADC3_IN5/FG3
20 PF8/ADC3_IN6/FG3
21 PF9/ADC3_IN7/FG3
22 PF10/ADC3_IN8/FG3
23 PH0/XTAL_IN
24 PH1/XTAL_OUT
25 NRST
26 PC0/ADC123_IN10/CMP3_INP4/FG2
27 PC1/ADC123_IN11/FG3
28 PC2/ADC123_IN12/FG3
29 PC3/ADC123_IN13/CMP1_INM4/FG2
30 VCC
31 AVSS_VREFL
32 VREFH
33 AVCC
34 PA0/ADC123_IN0/PGA_1/SH_1/FG2
35 PA1/ADC123_IN1/PGA_2/SH_2/FG2
36 PA2/ADC123_IN2/PGA_3/SH_3/FG2
37 PA3/ADC123_IN3/PGA123_VSS/CMP1_INP
38 AVSS
39 AVCC
40 PA4/ADC12_IN4/DAC1_OUT1/CMP2_INP
41 PA5/ADC12_IN5/DAC1_OUT2/CMP2_INP
42 PA6/ADC12_IN6/PGA_4/CMP1_INP2
43 PA7/ADC12_IN7/PGA4_VSS/CMP123_INM
44 PC4/ADC12_IN14/DAC2_OUT1/CMP2_INM
45 PC5/ADC12_IN15/DAC2_OUT2/CMP3_INM
46 PB0/ADC12_IN8/CMP3_INP2/I
47 PB1/ADC12_IN9/CMP3_INP3/I
48 PB2/PVD2EXINP/F
49 PF11/FG
50 PF12/FG
51 VSS
52 VCC
53 PF13/FG
54 PF14/FG
55 PF15/FG
56 PG0/FG
57 PG1/FG
58 PE7/FG
59 PE8/FG
60 PE9/FG
61 VSS
62 VCC
63 PE10/CMP1_INP3/F
64 PE11/FG
65 PE12/CMP4_INM3/F
66 PE13/CMP4_INM4/F
67 PE14/CMP4_INP3/F
68 PE15/CMP4_INP4/F
69 PB10/FG
70 PB11/FG
71 VCAP_
72 VCC
73 PB12/FG1
74 PB13/FG1
75 PB14/USBHS_DM/FG1
76 PB15/USBHS_DP/FG1
77 PD8/FG1
78 PD9/FG1
79 PD10/FG1
80 PD11/FG1
81 PD12/FG3
82 PD13/FG3
83 VSS
84 VCC
85 PD14/FG3
86 PD15/FG3
87 PG2/FG3
88 PG3/FG3
89 PG4/FG3
90 PG5/FG3
91 PG6/FG3
92 PG7/FG3
93 PG8/FG3
94 VSS
95 VCC
96 PC6/FG3
97 PC7/FG3
98 PC8/FG2
99 PC9/FG2
100 PA8/FG2
101 PA9/FG2
102 PA10/FG2
103 PA11/USBFS_DM/FG2
104 PA12/USBFS_DP/FG2
105 PA13/JTMS_SWDIO/FG2
106 VCAP_2
107 VSS
108 VCC
109 PA14/JTCK_SWCLK/FC
110 PA15/JTDI/FG1
111 PC10/FG3
112 PC11/FG3
113 PC12/FG3
114 PD0/FG3
115 PD1/FG3
116 PD2/FG3
117 PD3/FG3
118 PD4/FG2
119 PD5/FG2
120 VSS
121 VCC
122 PD6/FG2
123 PD7/FG2
124 PG9/FG2
125 PG10/FG2
126 PG11/FG2
127 PG12/FG2
128 PG13/FG2
129 PG14/FG2
130 VSS
131 VCC
132 PG15/FG1
133 PB3/JTDO_TRACESWC
134 PB4/NJTRST/FG1
135 PB5/FG1
136 PB6/FG1
137 PB7/FG1
138 PI13/MD
139 PB8/FG1
140 PB9/FG1
141 PE0/FG1
142 PE1/FG1
143 PI12/FG1
144 VCC

LQPF100


VCC 100
VSS 99
PE1/FG1 98
PE0/FG1 97
PB9/FG1 96
PB8/FG1 95
PI13/MD 94
PB7/FG1 93
PB6/FG1 92
PB5/FG1 91
PB4/NJTRST/FG1 90
PB3/JTDO_TRACESWO 89
PD7/FG2 88
PD6/FG2 87
PD5/FG2 86
PD4/FG2 85
PD3/FG3 84
PD2/FG3 83
PD1/FG3 82
PD0/FG3 81
PC12/FG3 80
PC11/FG3 79
PC10/FG3 78
PA15/JTDI/FG1 77
PA14/JTCK_SWCLK/FG 76
PE2/FG2 1
PE3/FG2 2
PE4/FG2 3
PE5/FG2 4
PE6/FG2 5
VBAT 6
PC13/RTCIO 7
PC14/XTAL32_OUT 8
PC15/XTAL32_IN 9
VSS 10
VCC 11
PH0/XTAL_IN 12
PH1/XTAL_OUT 13
NRST 14
PC0/ADC123_IN10/CMP3_INP4/FG3 15
PC1/ADC123_IN11/FG3 16
PC2/ADC123_IN12/FG3 17
PC3/ADC123_IN13/CMP1_INM4/FG3 18
VCC 19
AVSS_VREFL 20
VREFH 21
AVCC 22
PA0/ADC123_IN0/PGA_1/SH_1/FG2 23
PA1/ADC123_IN1/PGA_2/SH_2/FG2 24
PA2/ADC123_IN2/PGA_3/SH_3/FG2 25
75 VCC
74 VSS
73 VCAP_2
72 PA13/JTMS_SWDIO/FG2
71 PA12/USBFS_DP/FG2
70 PA11/USBFS_DM/FG2
69 PA10/FG2
68 PA9/FG2
67 PA8/FG2
66 PC9/FG2
65 PC8/FG2
64 PC7/FG3
63 PC6/FG3
62 PD15/FG3
61 PD14/FG3
60 PD13/FG3
59 PD12/FG3
58 PD11/FG1
57 PD10/FG1
56 PD9/FG1
55 PD8/FG1
54 PB15/USBHS_DP/FG1
53 PB14/USBHS_DM/FG1
52 PB13/FG1
51 PB12/FG1
26 PA3/ADC123_IN3/PGA123_VSS/CMP1_INP
27 AVSS
28 AVCC
29 PA4/ADC12_IN4/DAC1_OUT1/CMP2_INP
30 PA5/ADC12_IN5/DAC1_OUT2/CMP2_INP
31 PA6/ADC12_IN6/PGA_4/CMP1_INP2
32 PA7/ADC12_IN7/PGA4_VSS/CMP123_INM
33 PC4/ADC12_IN14/DAC2_OUT1/CMP2_INM
34 PC5/ADC12_IN15/DAC2_OUT2/CMP3_INM
35 PB0/ADC12_IN8/CMP3_INP2/F
36 PB1/ADC12_IN9/CMP3_INP3/F
37 PB2/PVD2EXINP/F
38 PE7/FG
39 PE8/FG
40 PE9/FG
41 PE10/CMP1_INP3/F
42 PE11/FG
43 PE12/CMP4_INM3/F
44 PE13/CMP4_INM4/F
45 PE14/CMP4_INP3/F
46 PE15/CMP4_INP4/F
47 PB10/FG
48 PB11/FG
49 VCAP_1
50 VCC

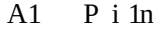
VFBGA176

Top View



A1 Pin

TFBGA208
Top View



A1 Pin

2-1

2.2

LQFP 176	LQFP 144	LQFP 100	VFBGA 176	TFBGA 208	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	) X Q F	) X Q F	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
									GPO		TIM4	TIM6	7 , 0 $	7 , 0 $	EMB,TIM6,TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2,TIM4	I2S	SPI,QSPI	SPI	USART		Communication Function Group
1	1	1	A2	R14	PE2		EIRQ2	TRACECLK		FCMREF	TIM4_3M		TIMA_9_M1 / TIMA_CLKA		TIMA_4G	USART3K				ETH_MIIXD3	EXMC_AD23			EVENTO		I2S3_M				FG2
2	2	2	A1	D5	PE3		EIRQ3	TRACED0					TIMA_9_M2 / TIMA_CLKB	TIMA_4WM1 / TI_4_CLK		USART6K				ETH_MIIIXD1	EXMC_AD19			EVENTC	TIM2_1A	I2S4_S	SPI2_N			FG2
3	3	3	B1	D6	PE4		EIRQ4	TRACED1					TIMA_9_M3	TIMA_4WM2 / TI_4_CLK		USART6TS					EXMC_AD20	ADVP_DA3	EI								

LQFP 176	LQFP 144	LQFP 100	VFBGA 176	TFBGA 208	Pin Name	Analog	EIRQ/WKUP	TRACE / JTAG	Func0 GPO	Func1	Func2	Func3	) X Q F	) X Q F	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63

LQFP176	LQFP144	LQFP100	VFBGA176	TFBGA208	Pin Name	Analog	EIRQ/WKUP	TRACE/JTAG	Func0	Func1	Func2	Func3	) X Q F	) X Q F	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
									GPO		TIM4	TIM6	7 , 0 $	7 , 0 $	EMB,TIM6,TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2,TIM4	I2S	SPI,QSPI	SPI	USART		Communication Function Group
77	67	45	P11	F12	PE14	CMP4_IN	EIRQ14				TIM4_1	TIM6_4MA	TIMA_1M4	TIMA_3WM4				SDIO1_	USBHS_PI_D1		EXMC_DA11			EVENTC	TIM2_2MA/TRI	I2S4_E	SPI1_N				FG3
78	68	46	R11	R6	PE15	CMP4_IN	EIRQ15				TIM4_1	TIM6_T	TIMA_7_M4	TIMA_5IG	EMBP_ORT	USART1K		SDIO1_	USBHS_PI_D2		EXMC_DA12			EVENTC	TIM2_2MB/TRI	I2S4_M					FG3
79	69	47	R12	P7	PB10		EIRQ10			ADTRG2	TIM4_2	TIM6_4MB	TIMA_2_M3	TIMA_1WM4				SDIO1_	USBHS_PI_D3	ETH_MIXER			EVNTP2	EVENTC		I2S3_E	QSPI_I	SPI2_S			FG3
80	70	48	R13	H12	PB11		EIRQ11				TIM4_1M		TIMA_2_M4		EMBP_ORT				USBHS_PI_D4	ETH_MIIMI_TX			EVNTP2	EVENTC							FG3
81	71	49	M10	K5	VCAP_1																										
-	-	-	-	L8	VSS																										
82	72	50	N10	L9	VCC																										
83	-	-	M11	N12	PH6		EIRQ6						TIMA_2_M3			USART5TS				ETH_MIIXD2	EXMC_CD	VP_DA8		EVENTC	TIM2_2MA/TRI						FG2
84	-	-	N12	N13	PH7		EIRQ7						TIMA_2_M2/TIMACLKB			USART5S				ETH_MIIXD3	EXMC_AD	VP_DA9		EVENTC							FG2
85	-	-	M12	H13	PH8		EIRQ8					TIM6_3MA	TIMA_2_M3			USART5K					EXMC_DA16	DVP_HSC		EVENTC			SPI5_N				FG2

LQFP 176	LQFP 144	LQFP 100	VFBGA 176	TFBGA 208	Pin

LQFP 176	LQFP 144	LQFP 100	VFBGA 176	TFBGA 208	Pin Name	Analog	EIRQ/WKUP	TRACE/ JTAG	Func0	Func1	Func2	Func3	) X Q F	) X Q F	Func6	Func7	Func8	Func9	Func10	Func11	Func12	Func13	Func14	Func15	Func16	Func17	Func18	Func19	Func20	Func21~31	Func32~63
									GPO		TIM4	TIM6	7 , 0 $	7 , 0 $	EMB,TIM6,TIMA	USART	KEY	SDIO	USBFS,USBHS,TIM2	ETH	EXMC,USBHS	DVP	EVNTPT	EVENTOUT	TIM2,TIM4	I2S	SPI,QSPI	SPI	USART		Communication Function Group
155	127	-	B8	C8	PG12		EIRQ12						TIMA_8_M2 / TIMA_CLKB			USART6S					EXMC_C			EVENTC							FG2
156	128	-	A8	B8	PG13		EIRQ13						TIMA_8_M3			USART6TS				ETH_MII_TXD24	EXMC_AD24	DVP_VSC		EVENTC							FG2
157	129	-	A7	R12	PG14		EIRQ14				TIM4_3M	TIM6_4MB	TIMA_8_M4							ETH_MII_TXD25	EXMC_AD25	DVP_DA2		EVENTC		I2S3_E					FG2
158	130	-	D7	G9	VSS																										
159	131	-	C7	D9	VCC																										
160	132	-	B7	A8	PG15		EIRQ15				TIM4_3MA	TIM6_4MA			TIMA_5G	USART6TS					EXMC_BA	DVP_DA13		EVENTC		I2S3_M					FG1
161	133	89	A10	D7	PB3		EIRQ3 + WKU	JTDO_WO		FCMREF	TIM4_3	TIM6_T	TIMA_2_M2 / TIMA_CLKB	TIMA_1_WM1 / TIM_12_CL				SDIO2_					ETNTP2	EVENTC							FG1
162	134	90	A9	C7	PB4		EIRQ4 + WKU	NJTRS			TIM4_3L	TIM6_3MB	TIMA_3_M1 / TIMA_CLKA	TIMA_1_WM2 / TIM_12_CL				SDIO1_				DVP_DA13	ETNTP2	EVENTC		I2S2_S					FG1
163	135	91	A6	B1	PB5		EIRQ5 + WKU			ADTRG3	TIM4_3H	TIM6_3MA	TIMA_3_M2 / TIMA_CLKB	TIMA_1_WM3	TIMA_1_IG			SDIO1_	USBHS_PI_D7	ETH_PPUT	EXMC_AD10	DVP_DA10	ETNTP2	EVENTC		I2S4_E	SPI3_N				FG1
164	136	92	B6	B7	PB6		EIRQ6 + WKU			ADTRG2	TIM4_3	TIM6_2MB	TIMA_4_M1 / TIMA_CLKA	TIMA_1_WM4	TIMA_1_WM1 / TI10_CLK			SDIO2_		ETH_MIIXCLK	EXMC_CD5	DVP_DA5	ETNTP2	EVENTC		I2S4_N	SPI3_N				FG1
165	137	93	B5	P11	PB7		EIRQ7 + WKU			ADTRG1	TIM4_3	TIM6_2MA	TIMA_4_M2 / TIMA_CLKB		TIMA_1_WM2 / TI10_CLK			SDIO1_		ETH_MIIXER	EXMC_AV	DVP_VSC	ETNTP2	EVENTC		I2S2_E	SPI3_N				FG1
166	138	94	D6	M9	PI13/MD											USART3X															
167	139	95	A5	A6	PB8		EIRQ8				TIM4_3	TIM6_1MB	TIMA_4_M3		TIMA_1_WM3	USART1K	KEYOUT	SDIO1_	USBFS_VVBUS	ETH_MIIXD3		DVP_DA6	ETNTP2	EVENTC	TIM2_3MA/ TRI	I2S2_N	SPI2_N				FG1
168	140	96	B4	A5	PB9		EIRQ9				TIM4_3	TIM6_1MA	TIMA_4_M4	TIMA_6IG	TIMA_1_WM4	USART1TS	KEYOUT	SDIO1_		ETH_MIIXD2		DVP_DA7	ETNTP2	EVENTC	TIM2_3MB/ TRI	I2S2_S	SPI2_N	SPI2_N			FG1
169	141	97	A4	G1	PE0		EIRQ0			MCO_1	TIM4_3		TIMA_4_G	TIMA_2G	USART1S					ETH_MIIMII_TX	EXMC_CD2	DVP_DA		EVENTC	TIM2_3A		SPI2_N		USART8X		FG1
170	142	98	A3	G2	PE1		EIRQ1			MCO_2	TIM4_3	TIM6_T		TIMA_1IG						ETH_MIIMII_TX	EXMC_CD3	DVP_DA		EVENTC	TIM2_3B		SPI2_N		USART8X		FG1
171	143	-	C6	A7	PI12		EIRQ12														EXMC_C										FG1
-	-	99	D5	G8	VSS																										
172	144	100	C5	E9	VCC																										
173	-	-	D4	C6	PI4		EIRQ4						TIMA_1_M1 / TIMA_CLKA		EMBP_ORT						EXMC_CD5	DVP_DA5		EVENTC							FG1
174	-	-	C4	C5	PI5		EIRQ5				TIM4_2	TIM6_5MA	TIMA_1_M2 / TIMA_CLKB								EXMC_CDC	DVP_VSC		EVENTC							FG1
175	-	-	C3	C4	PI6		EIRQ6				TIM4_2	TIM6_6MA	TIMA_1_M3								EXMC_DA28	DVP_DA6		EVENTC							FG1
176	-	-	C2	C3	PI7		EIRQ7				TIM4_2H	TIM6_7MA	TIMA_1_M4								EXMC_DA29	DVP_DA7		EVENTC							FG1
-	-	-	-	J5	AVCC																										
-	-	-	-	K3	VREFH																										
-	-	-	-	K4	AVSS_VREFL																										
-	-	-	-	L5	VSS																										
-	-	-	-	E11	VSS																										
-	-	-	-	J8	VSS																										

Package	Port Group	Bits																Pin Count	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Total
LQFP176	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	142
VFBGA176	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
TFBGA208	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortF	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortG	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortI	-	-	o	o	o	o	o	o	o	o	o	o	o	o	o	o	14	
LQFP144	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	116
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortF	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortG	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	2	
	PortI	-	-	o	o	-	-	-	-	-	-	-	-	-	-	-	-	2	
LQFP100	PortA	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	83
	PortB	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortC	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortD	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortE	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	o	16	
	PortH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	o	o	2	
	PortI	-	-	o	-	-	-	-	-	-	-	-	-	-	-	-	-	1	
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Port					5V
PortA	PA3~PA5 PA7~PA10 PA13~PA15			, ,	
	PA0,PA1,PA2, PA6,PA11,PA12			, ,	
PortB	PB0~PB13			, ,	
	PB14,PB15			, ,	
PortC	PC0~PC15			, ,	
PortD	PD0~PD15			, ,	
PortE	PE0~PE15			, ,	
PortF	PF0~PF15			, ,	
PortG	PG0~PG15			, ,	
PortH	PH0~PH15			, ,	
PortI	PI0~PI13			, ,	

2-4

– VREFH/ AVCC

	RTCICx (x=0~1)	I		
Timer2	TIM2_x_CLKA	I		
(x=1~4)	TIM2_x_CLKB	I		
	TIM2_x_PWMA/TRIGA	IO		PWM
	TIM2_x_PWMB/TRIGB	IO		PWM
Timer4	TIM4_x_CLK	I		
(x=1~3)	TIM4_x_OUH	IO	PWM	U
	TIM4_x_OUL	IO	PWM	U
	TIM4_x_OVH	IO	PWM	V
	TIM4_x_OVL	IO	PWM	V
	TIM4_x_OWH	IO	PWM	W

QSPI	QSPI_IOx (x=0~3)	IO	
	QSPI_SCK	O	
	QSPI_NSS	O	
I2Cx (x=1~6)	I2Cx_SCL	IO	
	I2Cx_SDA	IO	
I2Sx (x=1~4)	I2Sx_SD	IO	
	I2Sx_SDIN	I	
	I2Sx_WS	IO	
	I2Sx_CK	IO	
	I2Sx_EXCK	I	
	I2Sx_MCK	O	
CANx (x=1~2)	CANx_TX	O	
	CANx_RX	I	
SDIOx (x=1~2)	SDIOx_Dy (y=0~7)	IO	SD
	SDIOx_CK	O	SD
	SDIOx_CMD	IO	SD
	SDIOx_CD	I	SD
	SDIOx_WP	I	SD
USB_FS	USBFS_DM	IO	USBFS PHY D-
	USBFS_DP	IO	USBFS PHY D+
	USBFS_VBUS	I	USBFS VBUS
	USBFS_ID	I	USBFS ID
	USBFS_SOF	O	USBFS SOF
	USBFS_DRVVBUS	O	USBFS VBUS
USB_HS	USBHS_DP	IO	USBHS PHY D+
	USBHS_DM	IO	USBHS PHY D-
	USBHS_VBUS	I	USBHS VBUS
	USBHS_ID	I	USBHS ID
	USBHS_SOF	O	USBHS SOF
	USBHS_DRVVBUS	O	USBHS VBUS
	USBHS_ULPI_CLK	I	ULPI clock
	USBHS_ULPI_DIR	I	ULPI dir
	USBHS_ULPI_STP	O	ULPI stp
	USBHS_ULPI_NXT	I	ULPI nxt
	USBHS_ULPI_Dx (x=0~7)	IO	ULPI data

ETHMAC	ETH_SMI_MDC	O	SMI
	ETH_SMI_MDIO	IO	SMI
	ETH_PPS_OUT	IO	PPS
	ETH_MII_RMII_RXCLK	I	MII RMII
	ETH_MII_RMII_RXDV	I	MII RMII
	ETH_MII_RMII_RXD0	I	MII 0 RMII 0
	ETH_MII_RMII_RXD1	I	MII 1 RMII 1
	ETH_MII_RMII_TXEN	O	MII RMII
	ETH_MII_RMII_TXD0	O	MII 0 RMII 0
	ETH_MII_RMII_TXD1	O	MII 1 RMII 1
	ETH_MII_RXD2	I	MII 2
	ETH_MII_RXD3	I	MII 3
	ETH_MII_RXER	I	MII
	ETH_MII_TXCLK	I	MII
	ETH_MII_TXD2	O	MII 2
	ETH_MII_TXD3	O	MII 3
	ETH_MII_TXER	O	MII
	ETH_MII_COL	I	MII
	ETH_MII_CRS	I	MII
CMP	VCOUT1	O	CMP1
	VCOUT2	O	CMP2
	VCOUT3	O	CMP3
	VCOUT4	O	CMP4
	VCOUT	O	CMP1~4 OR
	CMPx_INPy (x=1~4 y=2~4)	I	CMPx
	CMPx_INM4 (x=1~4)	I	CMPx
	CMP123_INM3	I	CMP1,2,3
	CMP4_INM3	I	CMP4
ADC	ADTRG1	I	ADC1 AD
	ADTRG2	I	ADC2 AD
	ADTRG3	I	ADC3 AD
	ADC123_INx (x=0~3,10~13)	I	ADC1,2,3
	ADC12_INx (x=4~9,14,15)	I	ADC1,2
	ADC3_INx (x=4~9,14,15)	I	ADC3
	PGA123_VSS	I	PGA1~3 Ground

	PGA4_VSS	I	PGA4 Ground
DAC	DACx_OUTy (x=1,2 y=1,2)	O	DAC
DVP	DVP_HSYNC	I	
	DVP_VSYNC	I	
	DVP_PIXCLK	I	
	DVP_DATAx (x=0~13)	I	
EXMC	EXMC_CLK	IO	EXMC
	EXMC_OE	O	
	EXMC_WE	O	
	EXMC_CLE	O	
	EXMC_ALE	O	
	EXMC_BAA	O	
	EXMC_ADV	O	
	EXMC_CEx (x=0~7)	O	
	EXMC_RBx(x=0~7)	I	
	EXMC_ADDx (x=0~29)	IO	
	EXMC_DATAx (x=0~31)	IO	

2.4

VCC	1.8V~3.6V VSS
VSS	0V
VBAT	VCC 100nF
VCAP_x (x=1~2)	VSS
AVCC	VCC VCC
AVSS	VSS VSS
VREFL	AVSS AVSS
VREFH	AVCC ADC AVCC
PI13/MD	NRST 4.7kΩ VSS
NRST	VCC
Pxy (x=A~I y=0~15)	5V 5V 5V VCC VREFH/AVCC VCC /VSS

2-6

3 ECs

3.1

V_{SS}

3.1.1

3.1.2

T_A = 25 V_{CC} 3.3 V

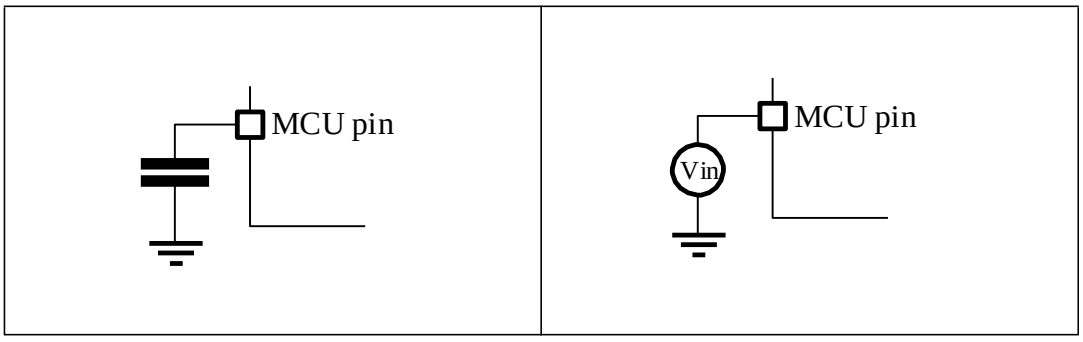
3.1.3

3.1.4

3-1

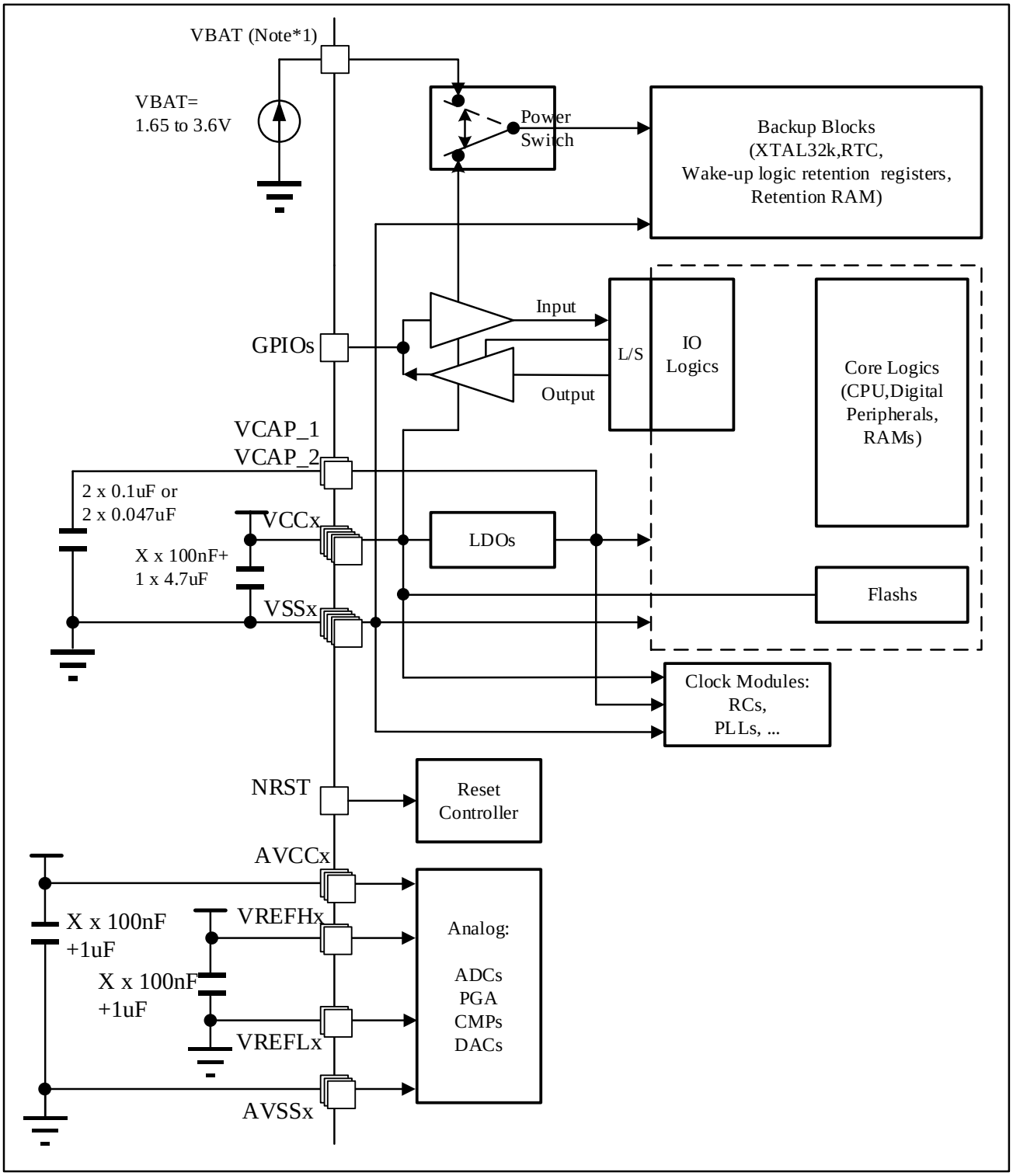
3.1.5

3-1



3-1 ( )

3.1.6



3-2

N o t e VBAT

1. 4.7μF VCC
2. AVSS = VSS

3.2

3-2 3-3 3-4

V_{CC}-V_{SS}	AVCCVCC VBAT(1)	-0.3	4.0	V
V_{IN}	PA11/USBFS_DP/SA_1D2M/USBFS_ PB14_USBHS_DP/SB_1D5M/_USBHS_ PA0PA1PA2PA6 (2)	V_{SS}-0.3	V_{CC}+4.0(5.8V)	
	PA11/USBFS_DP/SA_1D2M/USBFS_ PB14/USBHS_DP/SB_1D5M/USBHS_ PA0PA1PA2PA6	V_{SS}-0.3	Vc+c0.7(4.6V)	
$V_{ESD(HB}$	( )			-

3-2

1. VCCAVCCVBAT VSSAVSS

2. V_{IN} 3-3

ΣI_{VCC}	VCC	(1)	240	mA
ΣI_{VSS}	VSS	(1)	-240	
I_{VCC}	VCC	(1)	100	
I_{VSS}	VSS	(1)	-100	
I_{IO}	I/O		20	
	I/O		-20	
ΣI_{IO}	I/O		120	
	I/O		-120	

3-3

1. VCCAVCCVBAT VSSAVSS

T_{STG}		–65~150	°C
T_J		-40~125	°C

3-4

3.3

3.3.1

f_{HCLK}	AHB	(1) PWRC2.DVS=11 PWRC2.DDAS=1 PWRC3.DDAS=0	-	-	240	MHz
		PWRC2.DVS=10 PWRC2.DDAS= 0000	-	-	8	
V_{CC}		-	1.8	-	3.6	V
V_{AVCC}(2)		-	1.8	-	3.6	
V_{BAT}		-	1.6	-	3.6	
V_{IN}	5V (3)	2≤VCC≤3V.6 2≤VAVCC≤3V.6	–0.3	-	5.5	
		VCC<2V AVCC<2V	–0.3	-	5.2	
	PA11/USBFS_I PA12/USBFS_I PB14/USBHS_ PB15/USBHS_DP PA0 PA1 PA2 PA6	-	–0.3	-	V_{CC}+0.	

3-5

1.

2. VREFH 0 V_{AVCC}-V_{REFH}1.2 V

3. V_{CC}+0.3 /

3.3.2

T A

t_{VCC}	V C C	2 0	2 0 0 0 0	µ s / V
	V C C	2 0	2 0 0 0 0	

3-6 /

3.3.3

V_{BOR}	B O R	I C G 1 . B O R _ L E V	1 . 8 5	2 . 0 0	2 . 1 0	V
		I C G 1 . B O R _ L E V	1 . 9 6	2 . 1 0	2 . 2 0	V
		I C G 1 . B O R _ L E V	2 . 0 6	2 . 2 0	2 . 3 0	V
		I C G 1 . B O R _ L E V	2 . 1 7	2 . 4 0	2 . 5 0	V
V_{PVD}	P V D 1 (3)	P V D 1 L V L [2 : 0]	1 . 9 6	2 . 1 0	2 . 2 0	V
		P V D 1 L V L [2 : 0]	2 . 0 6	2 . 2 0	2 . 3 0	V
		P V D 1 L V L [2 : 0]	2 . 2 7	2 . 4 0	2 . 5 2	V
		P V D 1 L V L [2 : 0]	2 . 4 8	2 . 6 0	2 . 7 2	V
		P V D 1 L V L [2 : 0]	2.58	2 . 7 0	2.82	V
		P V D 1 L V L [2 : 0]	2.69	2 . 8 0	2.92	V
		P V D 1 L V L [2 : 0]	2.79	2 . 9 5	3.07	V
		P V D 1 L V L [2 : 0]	2.90(1)	3 . 0 5	3.17	V
V_{PVD2}	P V D 2 (3)	P V D 2 L V L [2 : 0]	2.06(1)	2.20	2.30	V
		P V D 2 L V L [2 : 0]	2.27	2.40	2.50	V
		P V D 2 L V L [2 : 0]	2.48	2.60	2.72	V
		P V D 2 L V L [2 : 0]	2.58	2 . 7 0	2.82	V
		P V D 2 L V L [2 : 0]	2.69	2 . 8 5	2.94	V
		P V D 2 L V L [2 : 0]	2.79	2 . 9 5	3.07	V
		P V D 2 L V L [2 : 0]	2.90(1)	3 . 0 5	3.17	V

		PVD2LVL[2:0]	1.(0)15	1.15	1.25	V
V_{pvhy}	PVD1,2(4)		-	100	-	mV
V_{POR}(1)	/	VPOR	1.60	1.68	1.80	V
		VPDR	1.56	1.64	1.76	V
V_{PORhy}	POR		-	40	-	mV
I_{RUSH}	(POR		-	160	200	mA
T_{NRST}	NRST		10	-	-	µs
T_{IPVD1}	PVD1		300	380	460	µs
T_{IPVD2}	PVD2		300	380	460	µs
T_{INRST}	NRST		25	35	50	µs
T_{RIPT}			140	160	200	µs
T_{RSTBO}	BOR		440	520	610	µs
T_{RSTP}			-	2500	3000	µs

3.3.4

I / O

I / O

3-3

F L A S H

1) I / O

2) f_{HCLK} 2 4 0 MHz / 1 2 0 MHz / 2 4 MHz

f_{HCLK} 8 MHz / 1 MHz

3) I C C _ R U N , I C C _ S L E E P , I C C _ S T P ,

I C C _ P D D h r y s t o n e I C C _ R D Y H S T O N E V B A T

I C C _ V B A T

4) O N / O F F

5) f_{HCLK} 2 4 0 MHz / 1 2 P0LMLHz

	3DUDPH	6\PERO		7D *f*&				8QL
					0LQ	7\S	0D[	
	f_{HCLK} 240MHz	ICC_RUN	while(1),OFF	-40	-	33	-	mA
			while(1),ON	-40	-	73	-	mA
		ICC_DHRYS	CACHE OFF	-40	-	37	-	mA
			CACHE ON	-40	-	38	-	mA
		ICC_SLEEP	OFF	-40	-	26	-	mA
			ON	-40	-	66	-	mA
		ICC_RUN	while(1),OFF	25	-	33	-	mA
			while(1),ON	25	-	74	-	mA
		ICC_DHRYS	CACHE OFF	25	-	38	-	mA
			CACHE ON	25	-	39	-	mA
		ICC_SLEEP	OFF	25	-	26	-	mA
			ON	25	-	67	-	mA
		ICC_RUN	while(1),OFF	85	-	-	70	mA
			while(1),ON	85	-	-	120	mA
		ICC_DHRYS	CACHE OFF	85	-	-	77	mA
			CACHE ON	85	-	-	78	mA
		ICC_SLEEP	OFF					

	3DUDPH	6\PERO		7D ƒ&				8QL
					0LQ	7\S	0D[	
	fHCLK 120 MHz	ICC_RUN	while(1),OFF	-40	-	21	-	mA
			while(1),ON	-40	-	42	-	mA
		ICC_DHRYST	CACHE OFF	-40	-	21	-	mA
			CACHE ON	-40	-	22	-	mA
		ICC_SLEEP	OFF	-40	-	16	-	mA
			ON	-40	-	37	-	mA
		ICC_RUN	while(1),OFF	25	-	22	-	mA
			while(1),ON	25	-	43	-	mA
		ICC_DHRYST	CACHE OFF	25	-	22	-	mA
			CACHE ON	25	-	23	-	mA
		ICC_SLEEP	OFF	25	-	16	-	mA
			ON	25	-	38	-	mA
		ICC_RUN	while(1),OFF	85	-	-	52	mA
			while(1),ON	85	-	-	78	mA
		ICC_DHRYST	CACHE OFF	85	-	-	53	mA
			CACHE ON	85	-	-	54	mA
		ICC_SLEEP	OFF	85	-	-	44	mA
			ON	85	-	-	71	mA
		ICC_RUN	while(1),OFF	105	-	-	84	mA
			while(1),ON	105	-	-	108	mA
		ICC_DHRYST	CACHE OFF	105	-	-	88	mA
			CACHE ON	105	-	-	89	mA
		ICC_SLEEP	OFF	105	-	-	77	mA
			ON	105	-	-	101	mA

3-9 2

1. Typ V_{CC}= 3.3 V
2. Max V_{CC}= 1.8 ~ 3.6 V
3.

	3DUDPH	6\PERO		7D f&			8QL
					0LQ	7\S	0D[	
	fHCLK 24 MHz	ICC_RUN	while(1),OFF	-40	-	6	-	mA
			while(1),ON	-40	-	13	-	mA
		ICC_DHRYST	CACHE OFF	-40	-	6	-	mA
		ICC_SLEEP	OFF	-40	-	4	-	mA
			ON	-40	-	12	-	mA
		ICC_RUN	while(1),OFF	25	-	6	-	mA
			while(1),ON	25	-	14	-	mA
		ICC_DHRYST	CACHE OFF	25	-	7	-	mA
		ICC_SLEEP	OFF	25	-	4	-	mA
			ON	25	-	13	-	mA
		ICC_RUN	while(1),OFF	85	-	-	27	mA
			while(1),ON	85	-	-	36	mA
		ICC_DHRYST	CACHE OFF	85	-	-	29	mA
		ICC_SLEEP	OFF	85	-	-	24	mA
			ON	85	-	-	33	mA
		ICC_RUN	while(1),OFF	105	-	-	54	mA
			while(1),ON	105	-	-	61	mA
		ICC_DHRYST	CACHE OFF	105	-	-	59	mA
		ICC_SLEEP	OFF	105	-	-	52	mA
			ON	105	-	-	59	mA

3-10 3

1. Typ V_{CC}= 3.3 V
2. Max V_{CC}= 1.8 ~ 3.6 V
3.

	3DUDPH	6\PERO		7D *f* &			8QL
					0LQ	7\S	0D[	
	f_{HCLK} 8 MHz	ICC_RUN	while(1),OFF	-40	-	3	-	mA
			while(1),ON	-40	-	6	-	mA
		ICC_DHRYS	CACHE OFF	-40	-	3	-	mA
		ICC_SLEEP	OFF	-40	-	2	-	mA
			ON	-40	-	6	-	mA
		ICC_RUN	while(1),OFF	25	-	3	-	mA
			while(1),ON	25	-	7	-	mA
		ICC_DHRYS	CACHE OFF	25	-	3	-	mA
		ICC_SLEEP	OFF	25	-	3	-	mA
			ON	25	-	7	-	mA
		ICC_RUN	while(1),OFF	85	-	-	22	mA
			while(1),ON	85	-	-	28	mA
		ICC_DHRYS	CACHE OFF	85	-	-	25	mA
		ICC_SLEEP	OFF	85	-	-	22	mA
			ON	85	-	-	27	mA
		ICC_RUN	while(1),OFF	105	-	-	48	mA
			while(1),ON	105	-	-	50	mA
		ICC_DHRYS	CACHE OFF	105	-	-	49	mA
		ICC_SLEEP	OFF	105	-	-	48	mA
			ON	105	-	-	50	mA

3-1 1 1

1. Typ V_{CC}= 3．3 V
2. Max V_{CC}= 1．8 ~ 3．6 V
3.

	3DUDPH	6\PERO		7D f&				8QL
					0LQ	7\S	0D[	
	fHCLK 1 MHz	ICC_RUN	while(1),OFF	-40	-	1	-	mA
			while(1),ON	-40	-	4	-	mA
		ICC_DHRYST	CACHE OFF	-40	-	2	-	mA
		ICC_SLEEP	OFF	-40	-	1	-	mA
			ON	-40	-	3	-	mA
		ICC_RUN	while(1),OFF	25	-	2	-	mA
			while(1),ON	25	-	4	-	mA
		ICC_DHRYST	CACHE OFF	25	-	2	-	mA
		ICC_SLEEP	OFF	25	-	2	-	mA
			ON	25	-	4	-	mA
		ICC_RUN	while(1),OFF	85	-	-	20	mA
			while(1),ON	85	-	-	24	mA
		ICC_DHRYST	CACHE OFF	85	-	-	23	mA
		ICC_SLEEP	OFF	85	-	-	20	mA
			ON	85	-	-	24	mA
		ICC_RUN	while(1),OFF	105	-	-	46	mA
			while(1),ON	105	-	-	47	mA
		ICC_DHRYST	CACHE OFF	105	-	-	47	mA
		ICC_SLEEP	OFF	105	-	-	46	mA
			ON	105	-	-	47	mA

3-12 2

1. Typ V_{CC}= 3.3 V
2. Max V_{CC}= 1.8 ~ 3.6 V
3.

	3DUDPI	6\PER	9&& 9	7D f&				8QL
					0LQ	7\S	0D[	
	-	ICC_S	PWC_PWRC1.STPDAS=	-40	-	191	-	uA
			PWC_PWRC1.STPDAS=	-40	-	56	-	uA
			PWC_PWRC1.STPDAS=	25	-	396	-	uA
			PWC_PWRC1.STPDAS=	25	-	248	-	uA
			PWC_PWRC1.STPDAS=	85	-	-	15	mA
			PWC_PWRC1.STPDAS=	85	-	-	16	mA
			PWC_PWRC1.STPDAS=	105	-	-	40	mA
			PWC_PWRC1.STPDAS(3)=	105	-	-	41	mA
	-	ICC_P	1	-40	-	9.1	-	uA
			2	-40	-	3.8	-	uA
			3	-40	-	1.6	-	uA
			4	-40	-	1.6	-	uA
			2+XTAL32+RTC	-40	-	5.1	-	uA
			2+LRC+RTC	-40	-	7.5	-	uA
			2+XTAL32+RTC+Back	-40	-	5.5	-	uA
			1	25	-	10.	-	uA
			2	25	-	4.3	-	uA
			3	25	-	2	-	uA
			4	25	-	2	-	uA
			2+XTAL32+RTC	25	-	5.8	-	uA
			2+LRC+RTC	25	-	8.1	-	uA
			2+XTAL32+RTC+Back	25	-	6.3	-	uA
			1	85	-	-	24	uA
			2	85	-	-	17	uA
			3	85	-	-	14	uA
			4	85	-	-	14	uA
			2+XTAL32+RTC	85	-	-	18	uA
			2+LRC+RTC	85	-	-		

	3DUDPI	6\PER	9&& 9	7D ƒ&			8QL
					0LQ	7\S	0D[	
			2+XTAL32+RTC+Back	85	-	-	23	uA
			1	105	-	-	75	uA
			2	105	-	-	68	uA
			3					

			RTCLRC	105	-	-	9.8	uA
			RTCLRCWKTM	105	-	-	9.9	uA

3-14

1. VBAT

3.3.5

CPU

- WFE
- WKUP VCC=3.3V

T_{STOP}		PWC_PWRC1.VHRCSD=1 PWC_PWRC1.VPLLSD=1 MRC RAM	2	5	us
T_{STOP}		MRC Flash	8	15	
T_{PD1}(1)	1	VCAP_1/VCAP_0 2.094uF 1uF	25	35	
		VCAP_1/VCAP_0 2.2uF 0.22uF	30	40	
T_{PD2}(1)	2	VCAP_1/VCAP_0 2.094uF 1uF	70	80	
		VCAP_1/VCAP_0 2.2uF 0.22uF	75	85	
T_{PD3}(1)	3	VCAP_1/VCAP_0 2.094uF 1uF	250	300	
		VCAP_1/VCAP_0 2.2uF 0.22uF	250	300	
T_{PD4}(1)	4				

3.3.6

3.3.6.1

XTAL I/O I/O

f_{XTAL_EXT}		-	1	-	25	MHz
V_{IH_XTAL}	XTAL_IN		0.8V_{CC}	-	V_{CC}	V
V_{IL_XTAL}	XTAL_IN		V_{SS}	-	0.2V_{CC}	
$t_{r(XTAL)}$ $t_{f(XTAL)}$	XTAL_IN		-	-	5	ns
$Duty_{(XTAL)}$		-	40	-	60	%

3-17

3.3.6.2

(X T A L) 4 25 MH z /

f_{XTAL_IN}			4	-	25	MHz
R_F(1)			-	300	-	kΩ
A_{XTAL}(2)	XTAL	-	-500	-	500	ppm
G_{mmax}	-		4	-	-	mA/
$t_{SU(XTAL)}$(3)		VCC = 8 MHz	-	-	2.0	ms
		VCC = 4 MHz	-	-	4.0	ms

3-18 XTAL-254MHz

1.

2.

3. $t_{SU(XTAL)}$ XTAL 8 MHz

3.3.6.3

3.3.7

3.3.7.1 +5&

f_{HRC}	(1)	1	-	16	-	MHz
		2	-	20	-	
		-	-	-	0.2	%
	(1)	TA=-40~105	-3(1)	-	3(1)	%
		TA=-20~105	-2.5	-	2.5	%
		TA=25	-1.5(1)	-	1.5(1)	%
$t_{st(HRC)}$	HRC	-	-	-	15	μs

3-20 HRC

1.

3.3.7.2 05&

f_{MRC}(1)		7.2(1)	8	8.8(1)	MHz
$t_{st(MRC)}$	MRC	-	-	3	μs

3-21 MRC

1.

3.3.7.3 /5&

f_{LRC}(1)		27.8(1)	32.7	37.6(1)	kHz
$t_{st(LRC)}$	LRC	-	-	36	μs

3-22 LRC

1.

3.3.7.4 6:'7 6:'7/5&

$f_{SWDTLRC}$(1)		9(1)	10	11(1)	kHz
tst(SWDTLRC)	SWDTLRC	-	-	57.	µs

3-23 SWDTLRC

1.

3.3.7.5 57& 57&5&

f_{RRC}(1)		29(.)1 5	32.7	36(1)	kHz
t sRRC(,)	RTRC	-	-	36	µs

3-24 RTCRC

1.

3.3.8 3//

			0LQ	7\S	0D[	8QL
f_{PLL_IN}	PLL PFD (Phase Fr Detector)(1) inp	-	1	-	25	MHz
f_{PLL_OUT}	PLL multipli	-	15	-	240	MHz
f_{VCO_OUT}	PLL VCO outp	-	240	-	480	MHz
Jitter	Period Jitte	PLL PFD input System clock= t-Peak	-	±10	-	ps
	Cyc-tl-Cycle Jit	PLL PFD input System clock= t-Peak	-	±150	-	
t_{LOCK}	PLL lock tim	-	-	80	120	µs

3-25 I 2-PSLLPLLA

			0LQ	7\S	0D[	8QL
f_{PLL_IN}	PLL PFD (Phas Detector)(1) inp	-	8	-	25	MHz
f_{PLL_OUT}	PLL multipli	-	37.	-	600	MHz
f_{VCO_OUT}	PLL VCO outp	-	600	-	120	MHz
Jitter	Period Jitte	PLL PFD input System clock= t-Peak	-	±70	-	ps
	Cyc-tl-Cycle Jit	PLL PFD input System clock= t-Peak	-	±100	-	
t_{LOCK}	PLL lock tim	-	-	80	120	µs

3-26 PLLPLLH

1. Jitter

3.3.9

I_{VCC}		V_{CC}= 1．8 V ~ 3．6 V	-	-	5	mA
		V_{CC}= 1．8 V ~ 3．6 V	-	-	10	
		V_{CC}= 1．8 V ~ 3．6 V	-	-	10	
		V_{CC}= 1．8 V ~ 3．6 V	-	-	10	

3-2 7

T_{prog}(1)			432 * T_{hclk}	484 * T_{hclk}	536 * T_{hclk}	μs
			122 * T_{hclk}	14+ 4 * T_{hclk}	16 + 6 * T_{hclk}	μs
T_{erase}(1)		-	16+ 2 * T_{hclk}	18+ 4 * T_{hclk}	206 * T_{hclk}	ms
T_{mass}(1)		-	16+ 2 * T_{hclk}	18+ 4 * T_{hclk}	206 * T_{hclk}	ms

3-2 8

1.

2. T_{hclk} CPU 1

N_{end}		T_A = 85	10	kcyc
N_{end}		T_A = 85	10	kcyc
T_{ret}		T_A = 85 after 10 kcy	10	Yea

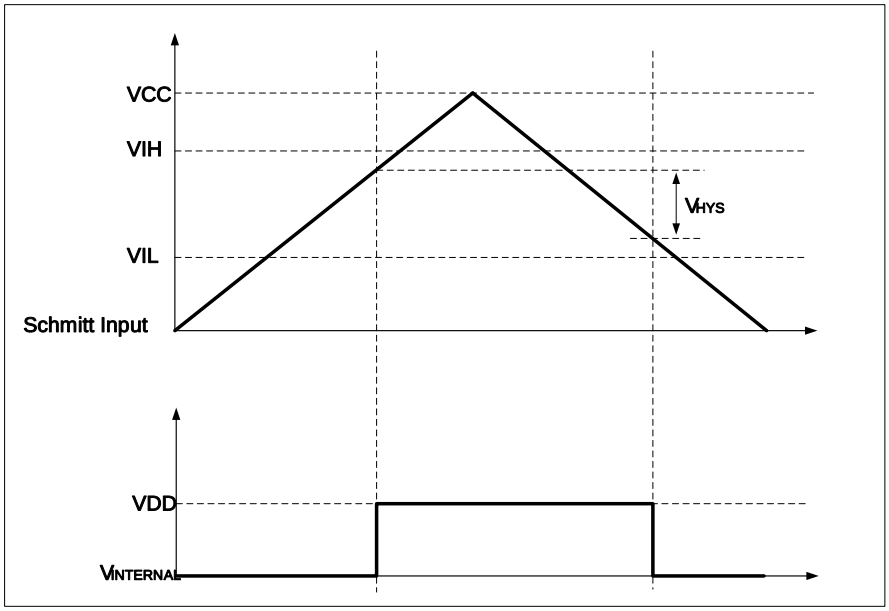
3-2 9

3.3.11 , 2

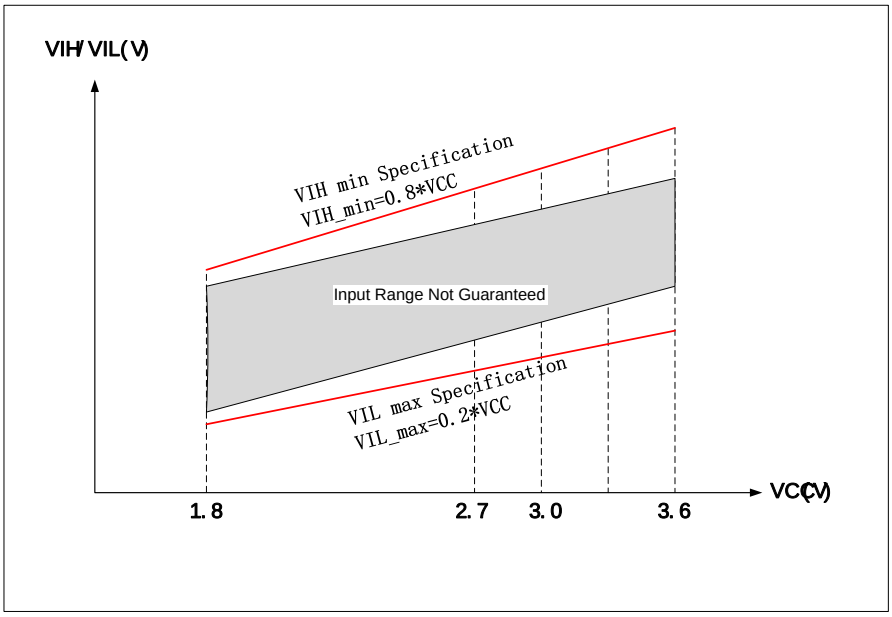
V_{IL}(1)	Schmitt	1.8V≤V_{CC}≤3.6	-	-	0.2V_{CC}	V
V_{IH}(1)	Schmitt	1.8V≤V_{CC}≤3.6	0.8V_{CC}	-	-	V
V_{HYS}	Schmitt	1.8V≤V_{CC}≤3.6	-	0.2	-	V
V_{IL}(1)	CMOS	1.8V≤V_{CC}≤3.6	-	-	0.3V_{CC}	V
V_{IH}(1)	CMOS	1.8V≤V_{CC}≤3.6	0.7V_{CC}	-	-	V
I_{LKG}(1)	I/O	V_{SS}≤V_{IN}≤V_{CC}	-	-	1	μA
		V_{IN}= 5(.25	-	-	10	μA

“USB ”

4. PA11/USBHPSA_12DMUSBHFSB_14DPUSBHPSB_15DMUSBHS_DP



3-6 Schmitt input DC electrical character



3-7 VIH/VIL versus VCC (Schmitt Input)

GPIO(/) ±20 mA

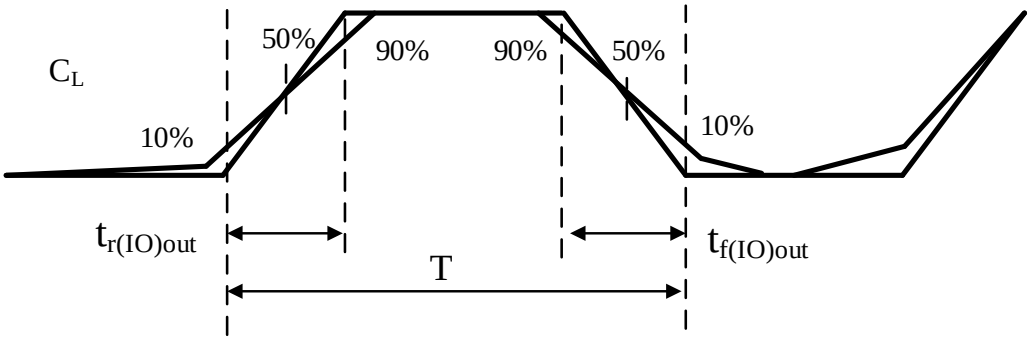
PC13 PC14 PC15 PI8 ∑IIO PC13

PC14 PC14 PI8 ≤ 200mA

	VOL(1)(2)		IIO=±1.5mA, 1.8V≤VCC≤2.7	-	-	0.6	
	VOH(1)(2)			VCC-0.4	-	-	
	VOL(1)(2)		IIO=±3mA, 2.7V≤VCC≤3.6	-	-	0.6	
	VOH(1)(2)			VCC-0.4	-	-	
	VOL(1)(2)		IIO=±6mA, 2.7V≤VCC≤3.6	-	-	1.3	
	VOH(1)(2)			VCC-1.3	-	-	
	VOL(1)(2)		IIO=±3mA, 1.8V≤VCC≤2.7	-	-	0.4	
	VOH(1)(2)			VCC-0.4	-	-	
	VOL(1)(2)		IIO=±5mA, 2.7V≤VCC≤3.6	-	-	0.4	V
	VOH(1)(2)			VCC-0.4	-	-	
	VOL(1)(2)		IIO=±20mA	-	-	1.3	

	f_{max}(IO)out	(1)	C_L=30pF, 2.7V≤VDD≤5.5V	-	-	20	MHz
			C_L=30pF, 1.8V≤VDD<2.7V	-	-	10	
			C_L=10pF, 2.7V≤VDD≤5.5V	-	-	40	
			C_L=10pF, 1.8V≤VDD<2.7V	-	-	20	
	t_f(IO)out t_r(IO)out		C_L=30pF, 2.7V≤VDD≤5.5V	-	-	15	ns
			C_L=30pF, 1.8V≤VDD<2.7V	-	-	25	
			C_L=10pF, 2.7V≤VDD≤5.5V	-	-	7.5	
			C_L=10pF, 1.8V≤VDD<2.7V	-	-	15	
	f_{max}(IO)out	(1)	C_L=30pF, 2.7V≤VDD≤5.5V	-	-	45	MHz
			C_L=30pF, 1.8V≤VDD<2.7V	-	-	22.	
			C_L=10pF, 2.7V≤VDD≤5.5V	-	-	90	
			C_L=10pF, 1.8V≤VDD<2.7V	-	-	45	
	t_f(IO)out t_r(IO)out		C_L=30pF, 2.7V≤VDD≤5.5V	-	-	6	ns
			C_L=30pF, 1.8V≤VDD<2.7V	-	-	10	
			C_L=10pF, 2.7V≤VDD≤5.5V	-	-	4	
			C_L=10pF, 1.8V≤VDD<2.7V	-	-	6	
	f_{max}(IO)out	(1)	C_L=30pF, 2.7V≤VDD≤5.5V	-	-	100	MHz
			C_L=30pF, 1.8V≤VDD<2.7V	-	-	50	
			C_L=10pF, 2.7V≤VDD≤5.5V	-	-	180	
			C_L=10pF, 1.8V≤VDD<2.7V	-	-	100	

1 0 p F



$(t_r + t_f)$ (2/3)T Duty cycle= 50%±5% C_L
/

3-8 I / O

3.3.12 +5 3 : 0

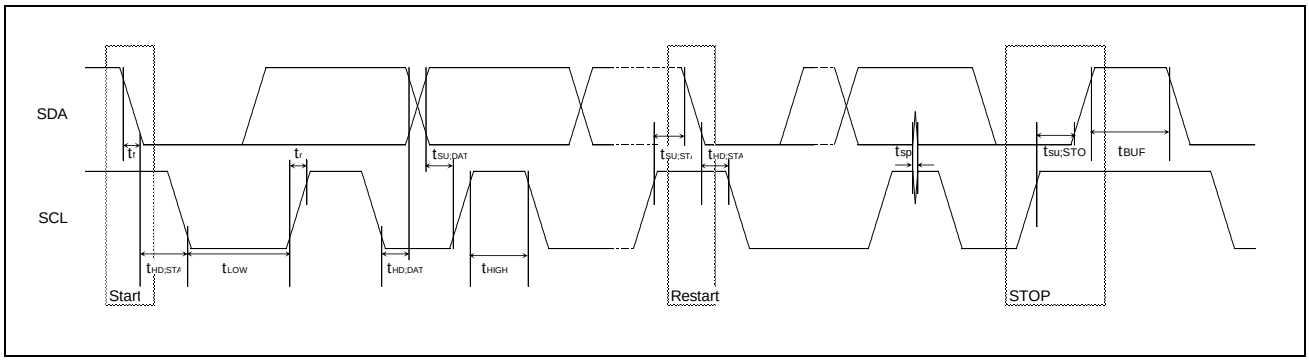
t _ h r p w m	H R P WM	-	5 0	-	p s

3-3 5 H R P WM

3.3.13 , &

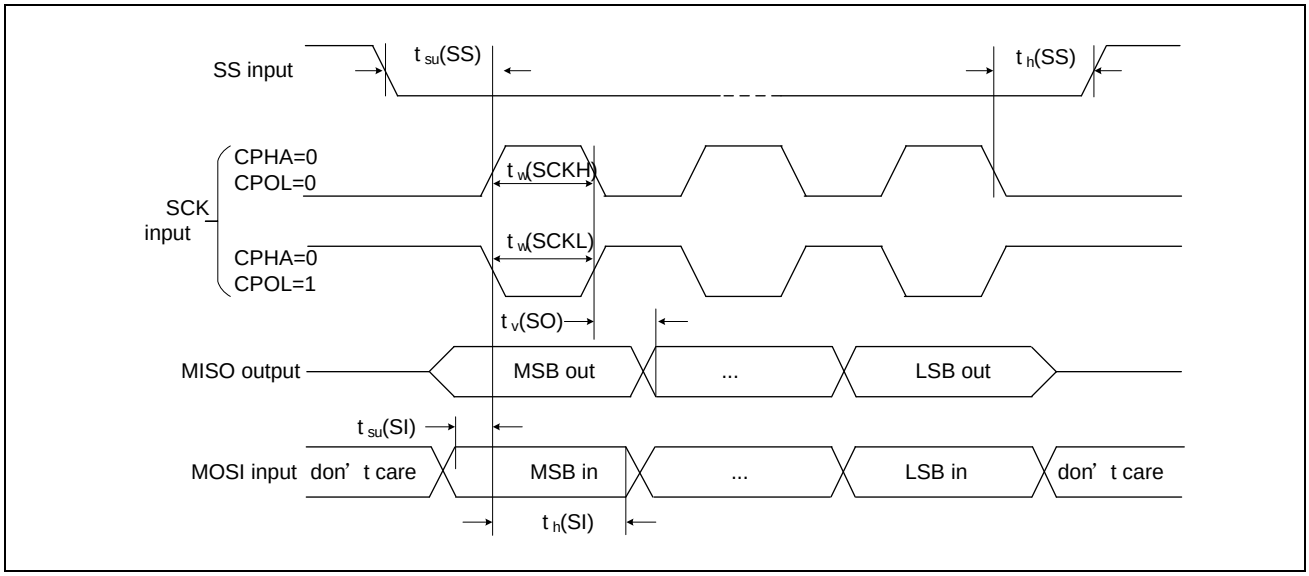
		60		)0		
		0LQ	0D[	0LQ	0D[	
f_{SCL}	SCL	0	100	0	400	kHz
$t_{HD;STA}$	/ Hol	4.0	-	0.6	-	us
t_{LOW}	SCL	4.7	-	1.3	-	us
t_{HIGH}	SCL	4	-	0.6	-	us
$t_{SU;STA}$	Setup	4.7	-	0.6	-	us
$t_{HD;DAT}$	Hold	0	-	0	-	us
$t_{SU;DAT}$	Setup	50+ t_{I2C}	-	50+ t_{I2C}	-	ns
t_R	SCL/SDA	-	1000	6.5	300	ns
t_F	SCL/SDA	-	300	6.5	300	ns
$t_{SU;STO}$	Setup	4	-	0.6	-	us
t_{BUF}	BUS	4.7	-	1.3	-	us
C_b		-	400	-	400	pF

3-3 6 I 2 C

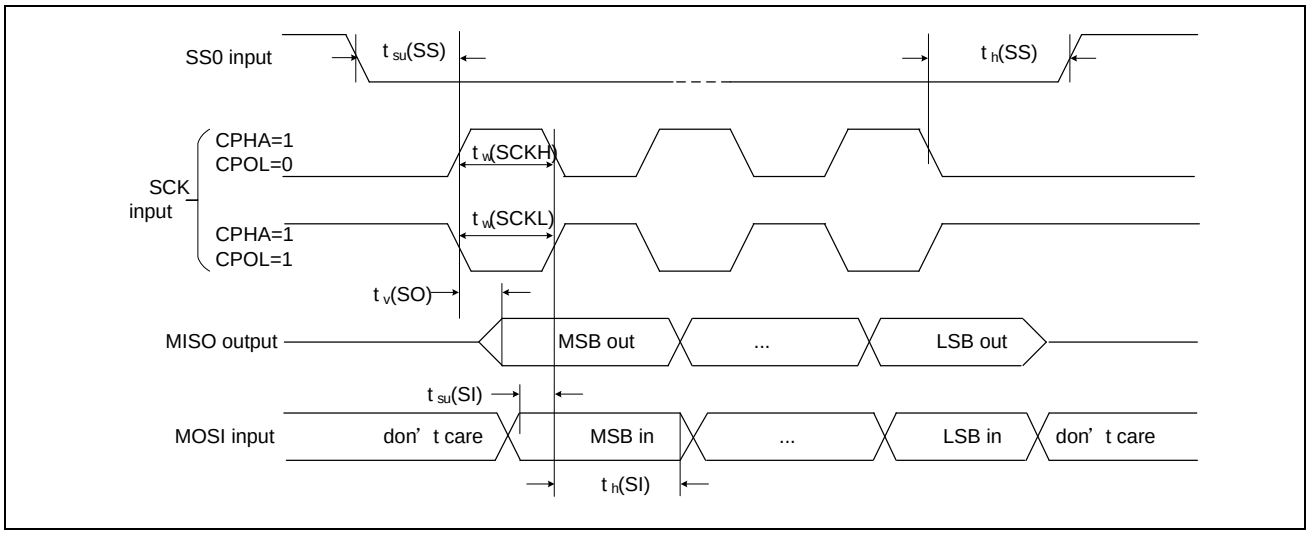


3-9 I 2 C

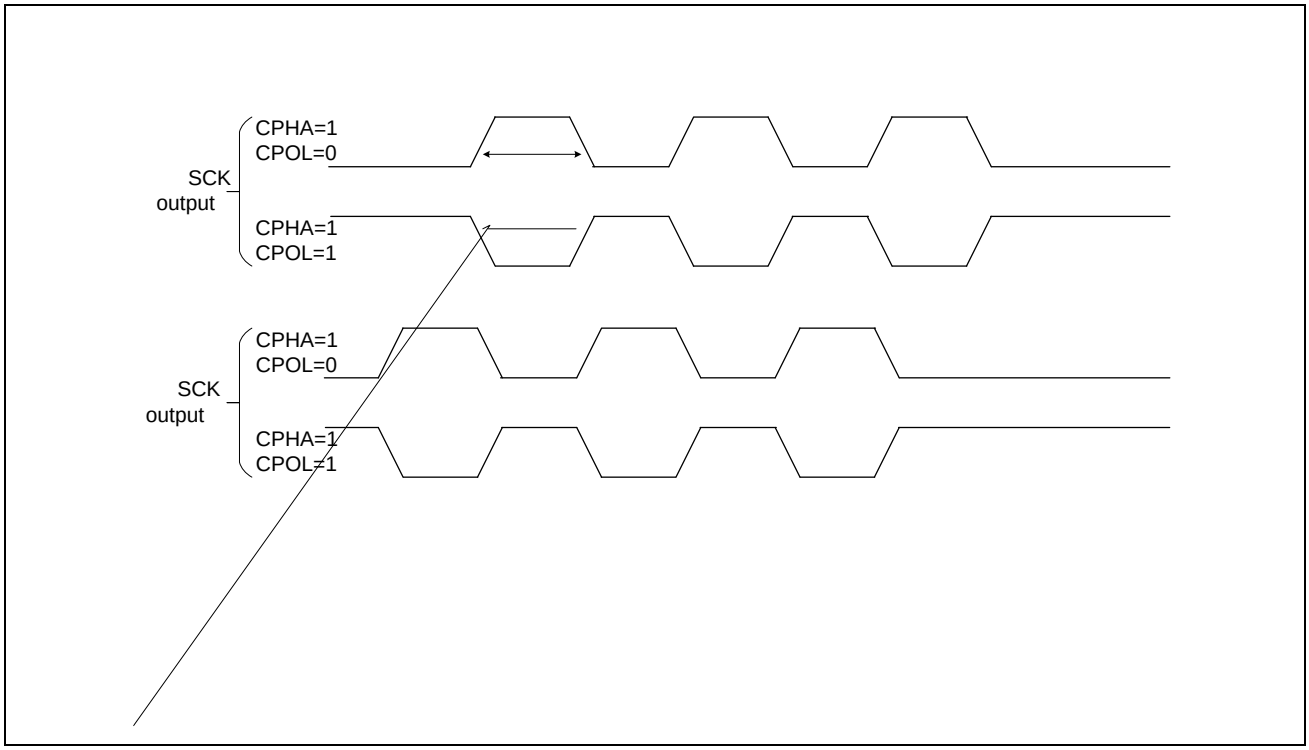
$t_{h(SS)}$	SS hold	slave mode 1.8V≤Vcc≤3.6V	6 T_{pclk1}	-	ns
		master mode 2.7V≤Vcc≤3.6V	-5 + NT_{sxxxk1} *1*3	-	ns
		master mode 1.8V≤Vcc<2.7V	-10 + N T_{sxxc} *1*3	-	ns



3-10 SPI timing diagram for master mode and CPHA=0



3-11 SPI timing diagram for master mode and CPHA=1

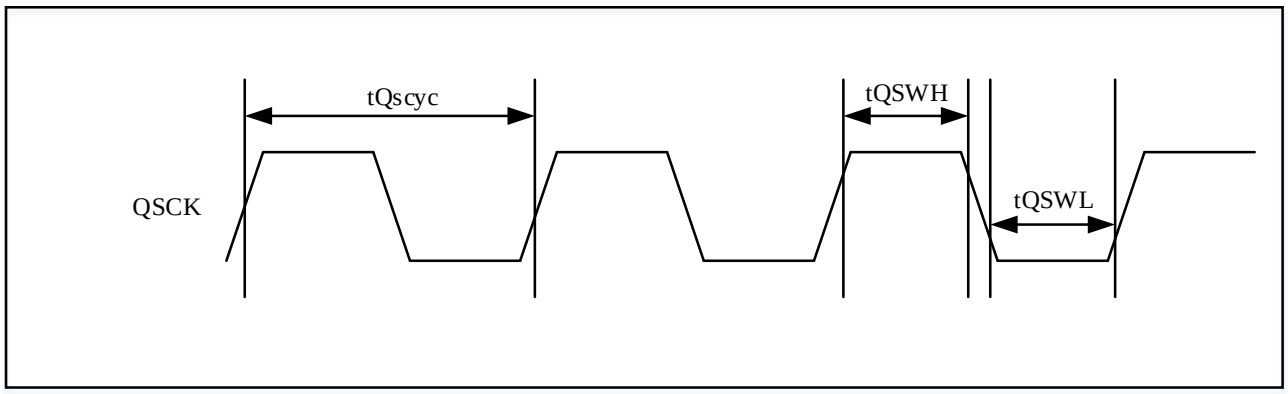


3-12 SPI timing diagram mode

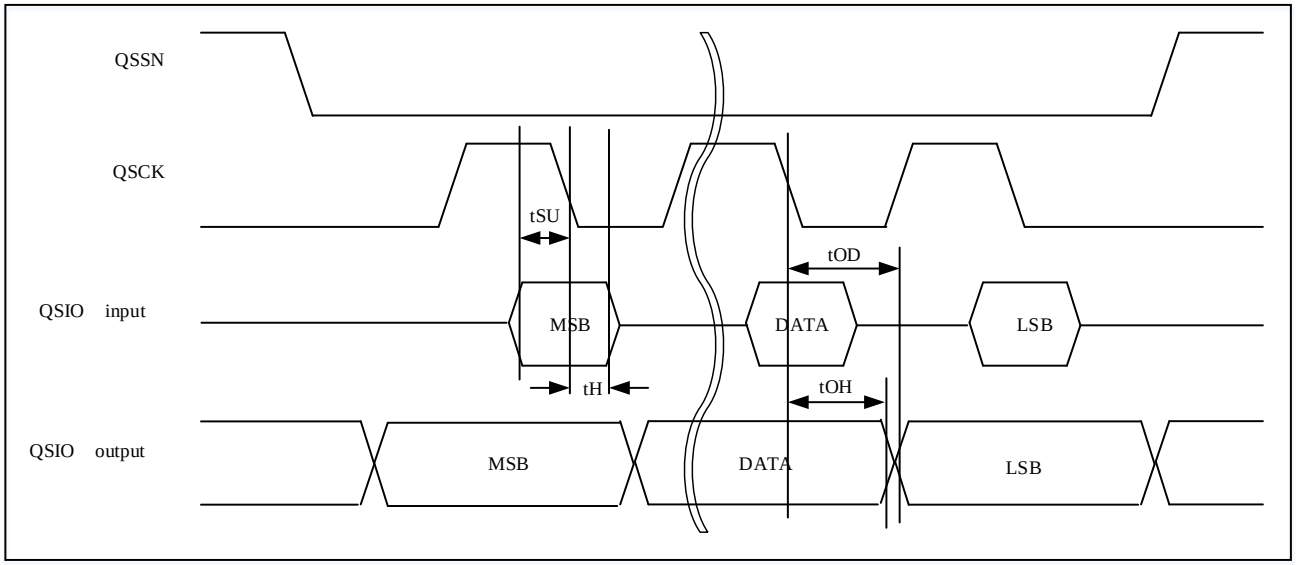
3.3.15 463,

t_{Qscyc}	QSPCK clock cycle	2	48	thclk
t_{QSWH}	QSPCK high level	t_{Qscyc}×0.4	-	ns
t_{QSWL}	QSPCK low level	t_{Qscyc}×0.4	-	ns
t_{SU}	data input setup time 2.7V~3.6V	5	-	ns
	data input setup time 1.8V~2.7V	5		ns
t_{IH}	data input hold time 2.7V~3.6V	11	-	ns
	data input hold time 1.8V~2.7V	15		ns
t_{OD}	data output delay	-	4	ns
t_{OH}	data output hold time	0	-	ns

3-38 QSPI



3-1 3 Q S P C K



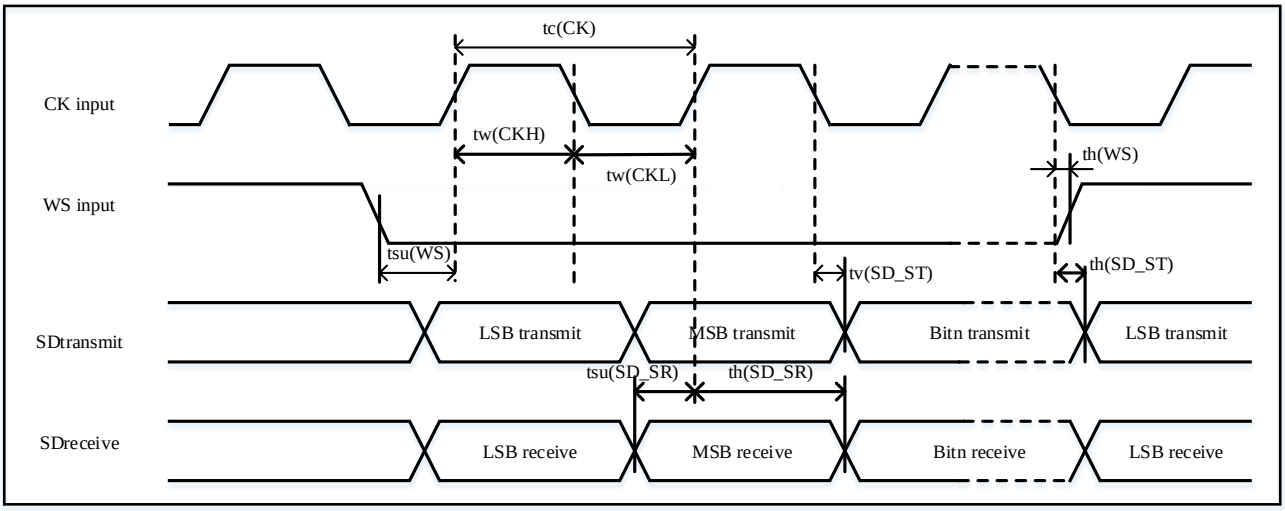
3-1 4 Q S P I

3.3.16 , 6

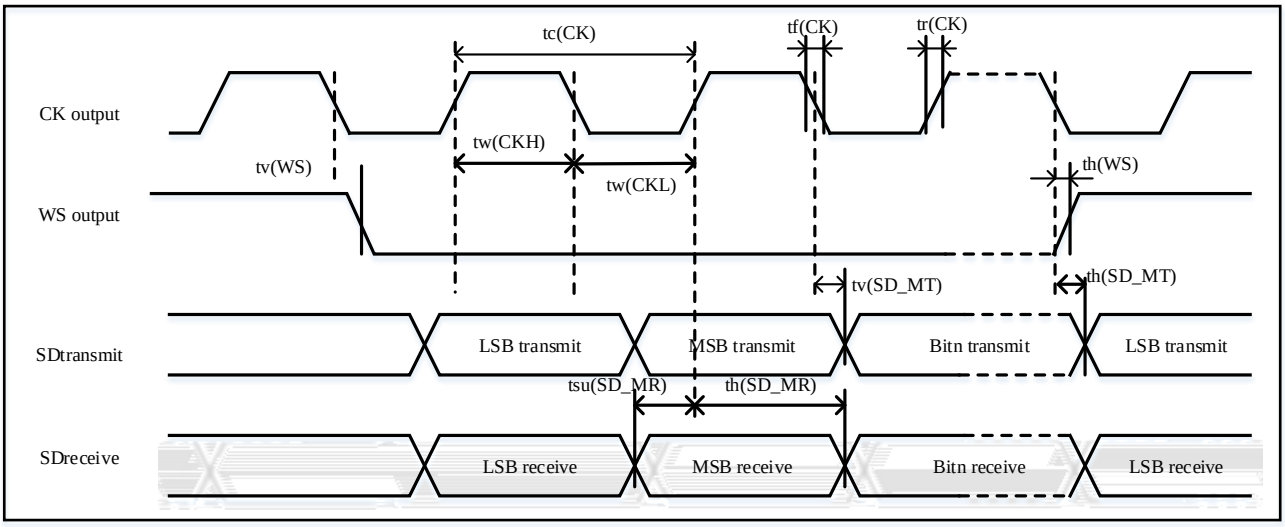
f_{MCK}	I2S main cl	-	256 *	256*	MHz
f_{CK}	I2S clock f	Master data: 3	20	64*F	MHz
		Slave data: 32	-	64*F	
D_{CK}	I2S clock f cycle	Slave receiver	30	70	%
t_v(WS)	WS valid ti	Master mode	-	6	ns
t_s(WS)	WSsetup tim	Slave mode	7.5	-	
t_h(WS)	WS hold tim	Slave mode	6	-	
t_s(SD_MR	Data input	Master r2e c7eVi~v3e	22	-	
		Master r1e c8eVi~v2e	25		
t_s(SD_SR		Slave receiver	7	-	
t_h(SD_MR	Data input	Master receive	0	-	
t_h(SD_SR		Slave receiver	7	-	
t_v(SD_ST) t_h(SD_ST)	Data output	Slave transmit edge)	-	24	
t_v(SD_MT)		Master transmi edge)	-	10	

3-39 I2S

1. FsI2S



3-15 I2S Philips



3-16 I2S Philips

3.3.17 &$1)' &$1 %

CANx_TX CANx_RX 3.13 I/O

3.3.18 86%

6\PERO		3DUDPHV	&RQGLWLRQ	0LQ	7\S	0D[	8QL
	V_{CC}		-	3.(2)	-	3.6	V
	V_{IL}		-	-	-	0.8	V
	V_{IH}		-	2.0	-	-	V
	V_{DI}		-	0.2	-	-	V
	V_{CM}		-	0.8	-	2.5	V
	V_{OL}		R_L= 1.Ω5k o (3 4.) 6 V	-	-	0.3	V
	V_{OH}		R_L= 1 Ω2k o (V4 S S	2.8	-	3.6	V
	V_{CRS}	Cr o-osvse r	C_L= 50pF	1.3	-	2.0	V
	t_R		C_L= 50pF 10%~90% oH-Vo of | V	4	-	20	ns
	t_F		C_L= 50pF 10%~90% oH-Vo of | V	4	-	20	ns
	t_{RFMA}	$t_R/_F t$	C_L= 50pF	90	-	111	%
R_{PD}			V_{IN} CVin host m	-	15.	-	kΩ
R_{PU}(3)			V_{IN} SVidle stat	0.90	1.2	1.57	kΩ
			V_{IN} SVin device	1.42	2.3	3.09	kΩ
Z_{DRV}		(5)	Driving high	28	36	44	Ω

3-40 USB -Sple ed

1.

2. 2.7V USB USB

2.73.0V$_{CC}$

3.

4. R_L USB

5. DP DM Driver

6. DP DM / PHY

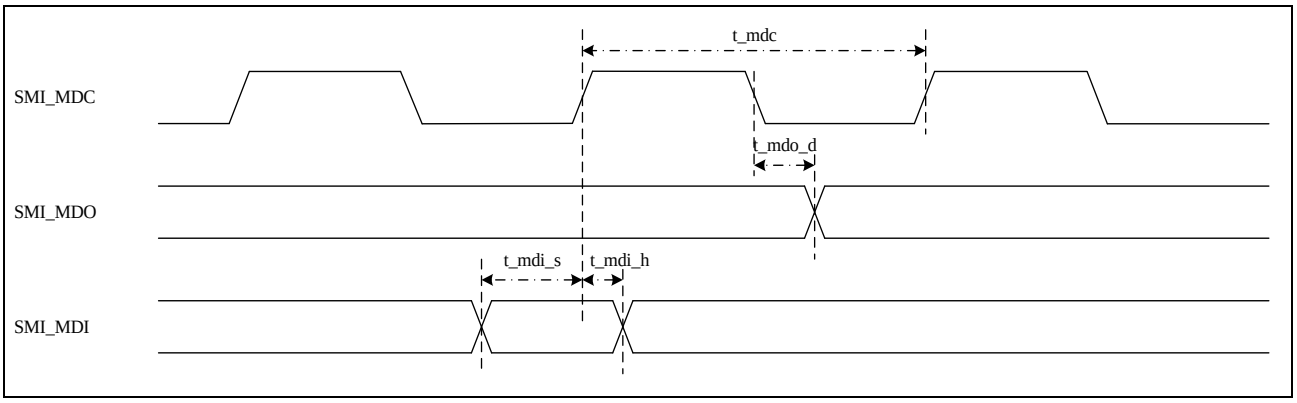
6\PERO		3DUDPHW	&RQGLWLRQ	0LQ	7\S	0D[	8QL
	V_{CC}		-	3.0(3)	-	3.6	V
	V_{IL}		-	-	-	0.8	V
	V_{IH}		-	2.0	-	-	V
	V_{DI}		-	0.2	-	-	V
	V_{CM}		-	0.8			

3.3.19 (7+0$&

3.3.19.1 60,

6\PERO	3DUDPHWHU	0LQ	7\S	0D[	8QL\
t_mdc	SMI_MDC	405	420	425	ns
t_mdo_d	SMI_MDO 2.7V~3.6V	-	-	Tpclk	ns
	SMI_MDO 1.8V~2.7V	-		Tpclk1	ns
t_mdi_s	SMI_MDISetup	11	-	-	ns
t_mdi_h	SMI_MDIHold	0	-	-	ns

3-43 ETHMAC_SMI

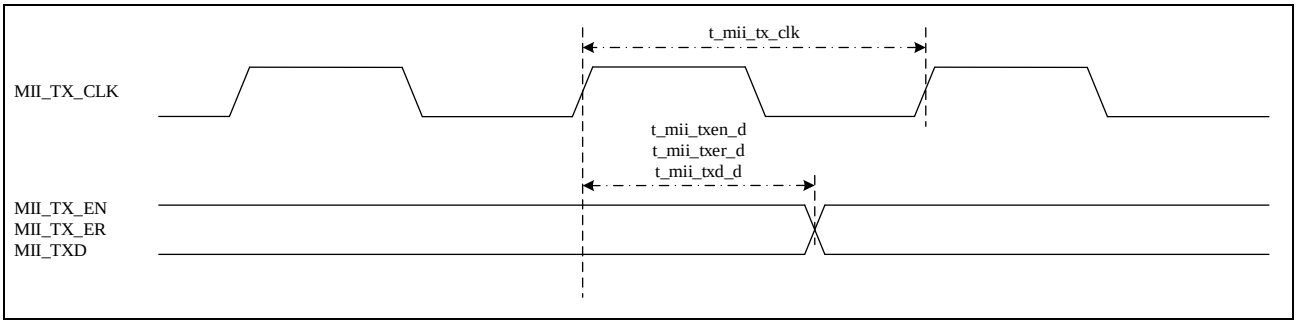


3-19 ETHMASCMI

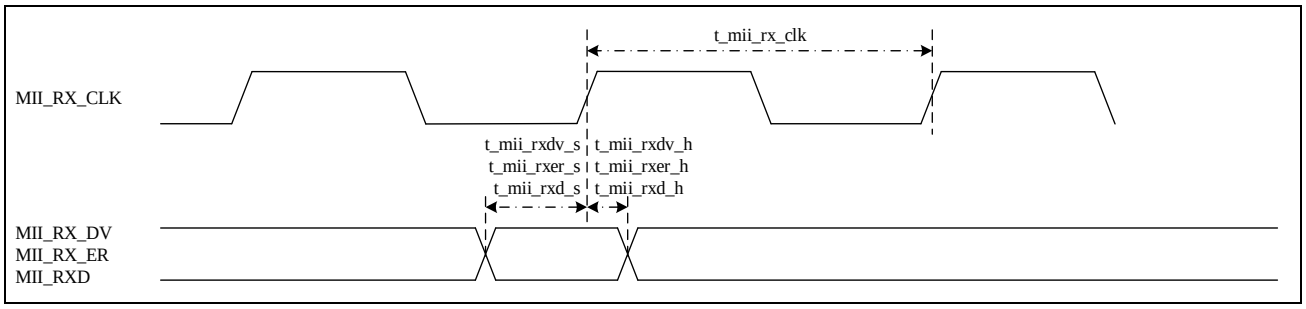
3.3.19.2 0, ,

6\PERO	3DUDPHWHU		0LQ	7\S	0D[	8QL
t_mii_tx_	MII_TX_CLK		-	40	-	ns
t_mii_txe	MII_TX_EN	2.7V~3.6V	5	-	15	ns
	MII_TX_EN	1.8V~2.7V	5		21	ns
t_mii_txe	MII_TX_ER	2.7V~3.6V	5	-	15	ns
	MII_TX_ER	1.8V~2.7V	5		21	ns
t_mii_txd_	MII_TXD	2.7V~3.6V	5	-	15	ns
	MII_TXD	1.8V~2.7V	5		21	ns
t_mii_rx_	MII_RX_CLK		-	40	-	ns
t_mii_rxd	MII_RX_DS	Vetup	8	-	-	ns
t_mii_rxd	MII_RX_DH	Vold	4	-	-	ns
t_mii_rxe	MII_RX_ES	Retup	8	-	-	ns
t_mii_rxe	MII_RX_EH	Rold	4	-	-	ns
t_mii_rxd_	MII_RXDS	etup	8	-	-	ns
t_mii_rxd_	MII_RXDH	old	4	-	-	ns

3-44 ETHMAC_MII



3-20 ETHMAC MII

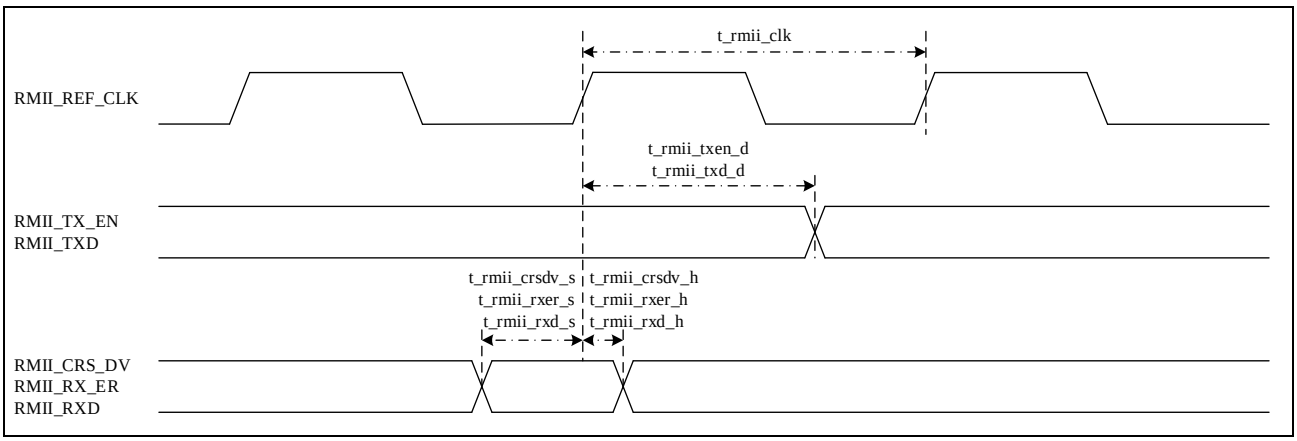


3-2 1 E T H MAMCI I

3.3.19.3 5 0, ,

6\PERO	3DUDPHWHU	0LQ	7\S	0D[	8QL
t_rmii_cl	RMII_REF_CLK	-	20	-	ns
t_rmii_tx	RMII_TX_EN 2.7V~3.6V	5	-	12.	ns
	RMII_TX_EN 1.8V~2.7V	5		15	ns
t_rmii_tx	RMII_TXD 2.7V~3.6V	5	-	12.	ns
	RMII_TXD 1.8V~2.7V	5		15	ns
t_rmii_cr	RMII_CRS_DV Setup	4	-	-	ns
t_rmii_cr	RMII_CRS_DV Hold	2	-	-	ns
t_rmii_rx	RMII_RX_ER Setup	4	-	-	ns
t_rmii_rx	RMII_RX_ER Hold	2	-	-	ns
t_rmii_rx	RMII_RXD Setup	4	-	-	ns
t_rmii_rx	RMII_RXD Hold	2	-	-	ns

3-4 5 E T H MA C_ R MI I



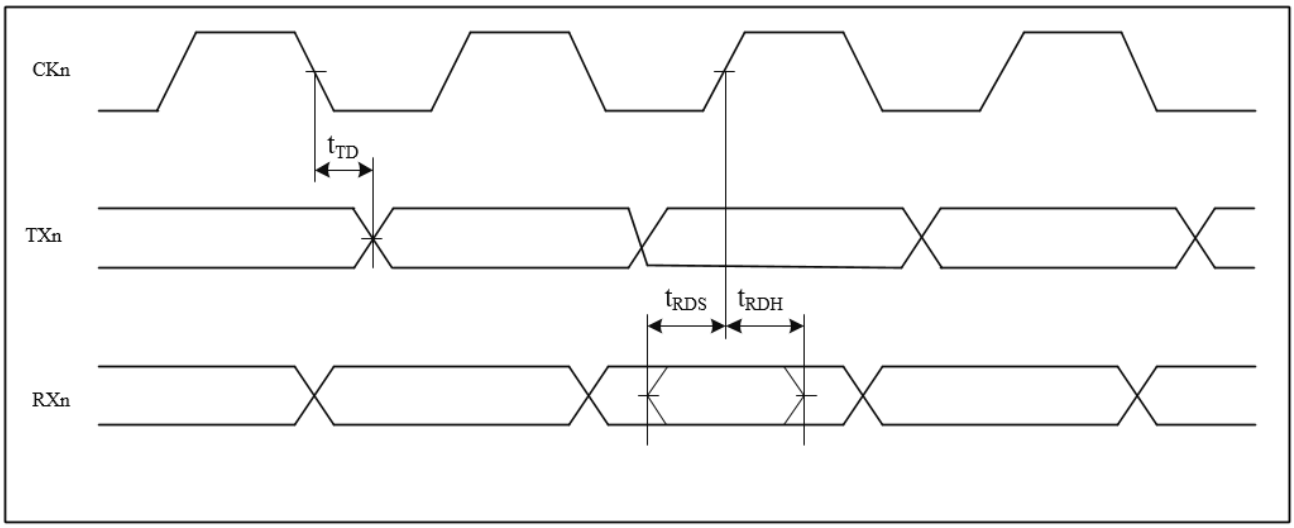
3-2 2 E T H MARCMI I

3.3.20 8 6 $ 5 7

t_{cyc}		UART	4	-	t_{PCLK1}
			6	-	
t_{CKw}			0.4	0.6	t_{cyc}
t_{CKr}			-	5	ns
t_{CKf}			-	5	ns
t_{TD}	2 . 7 V ≤ V c c ≤ 3 . 6		-	23	ns
	1.8V Vcc 2.7V		-	30	ns
t_{RDS}	2.7V Vcc 3.6V		17	-	ns
	1.8V Vcc 2.7V		23	-	ns
t_{RDH}			5	-	ns

3-4 6 U S A R T A C

UART		PCLK1/8
		PCLK1/32
2 . 3 V ≤ V c c ≤ 3 . 6 V		12.0Mbps

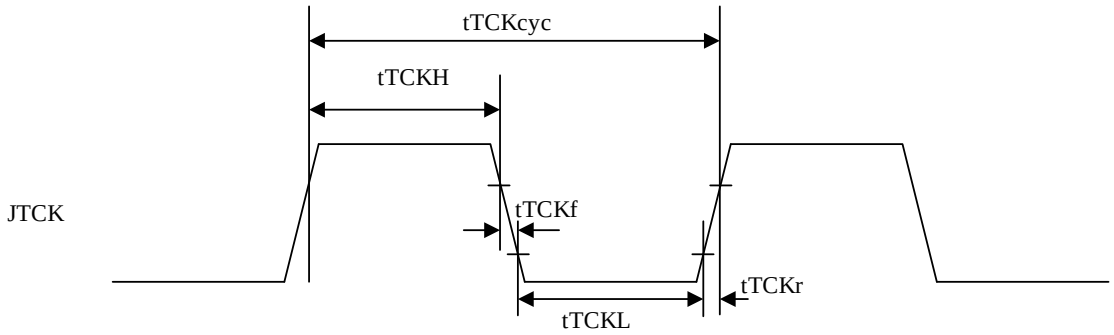


3-24 USART SPI

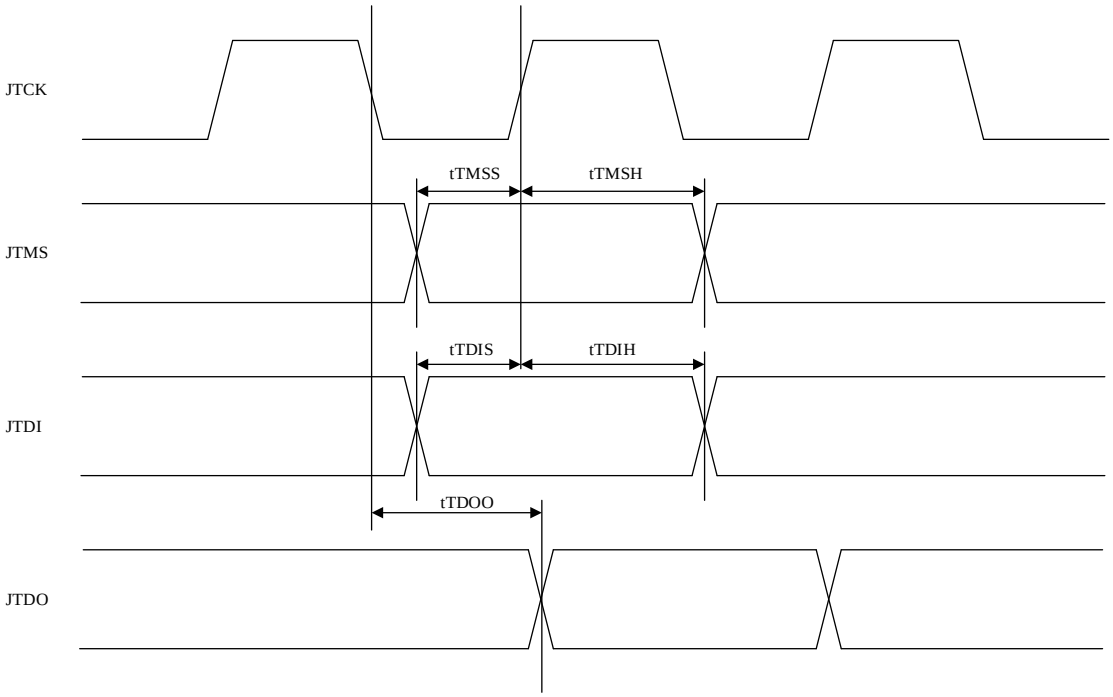
3.3.21 - 7$*

6\QER(	,WHP	0LQ	7\S	0D[	8QLW
t_{TCKcyc}	JTCK cdyocclke time	50	-	-	ns
t_{TCKH}	JTCK clock high p	15	-	-	ns
t_{TCKL}	JTCK clock low pu	15	-	-	ns
t_{TCKr}	JTCK clock rise t	-	-	5	ns
t_{TCKf}	JTCK clock fall t	-	-	5	ns
t_{TMSs}	JTMS setup time	10	-	-	ns
t_{TMSh}	JTMS hold time	10	-	-	ns
t_{TDIs}	JTDI setup time	10	-	-	ns
t_{TDIh}	JTDI hold time	10	-	-	ns
t_{TDOd}	JTDO data delay t	10	-	25	ns

3-48 JTAG



3-25 JTAG TCK

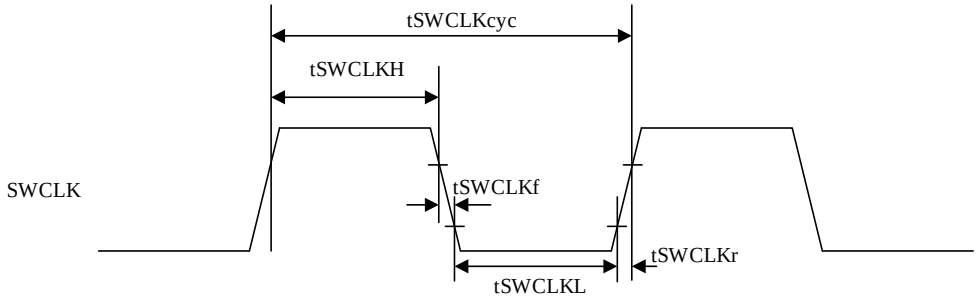


3-26 JTAG

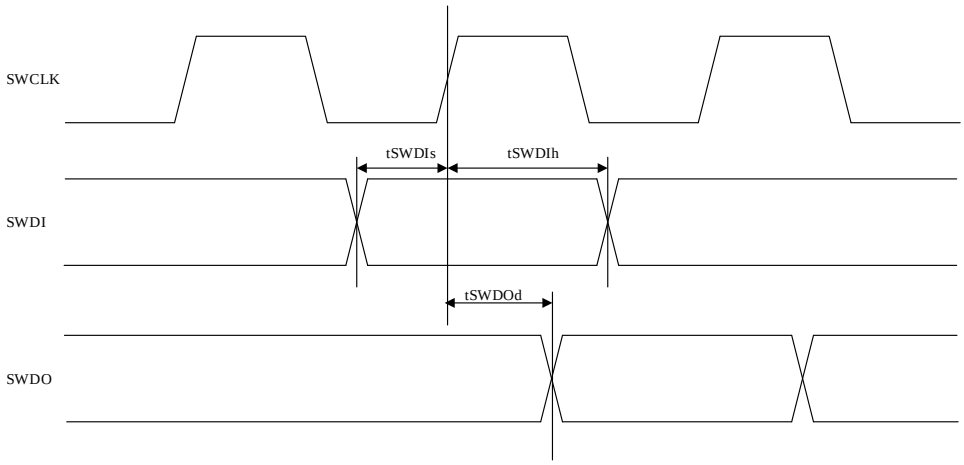
3.3.22 6:'

6\QER(	,WHP	0LQ	7\S	0D[	8QLW
$t_{SWCLKcyc}$	SWCLK clock cycle	50	-	-	ns
t_{SWCLKH}	SWCLK clock high	15	-	-	ns
t_{SWCLKL}	SWCLK clock low pulse width	15	-	-	ns
t_{SWCLKr}	SWCLK clock rise	-	-	5	ns
t_{SWCLKf}	SWLCK clock fall	-	-	5	ns
t_{SWDIs}	SWDI setup time	10	-	-	ns
t_{SWDIh}	SWDI hold time	10	-	-	ns
t_{SWDOd}	SWDO data delay t	10	-	25	ns

3-49 SWD



3-27 SWD SWCLK



3-28 SWDIO

3.3.23 （7 0

6\QER(	,WHP	0LQ	7\S	0D[	8QLW
$t_{TRCLKcyc}$	TRACECK clock cyc	20	-	-	ns
t_{TRCKH}	TRACECK clock hig	7	-	-	ns
t_{TRCKL}	TRACECK clock lov	7	-	-	ns
t_{TRCKr}	TRACECK clock ris	-	-	2.5	ns
t_{TRCKf}	TRACECK clock fal	-	-	2.5	ns
t_{TRD}	TRACED[3:0] output delay	1.6	-	8.4	ns

3.3.24 $ ' &

V_{AVCC}		-	1．8	-	3．6	V
$V_{REF(H1)}$		-	1．8	-	V_{AVCC}	V
f_{ADC}	ADC	V_{AVCC}≥2．4 ~3．	1	-	60	MHz
		V_{AVCC}≥1．8 ~2．	1	-	30	
			1	-	8	
V_{AIN}		-	V_{REFL}	-	V_{REFH}	V
R_{AIN}		1	-	-	50	kΩ
R_{ADC}		-	-	3	6	kΩ
C_{ADC}		-	-	4	7	Pf
t_D		f_{ADC}= 60 MHz	-	-	0．3	μs

3-51 ADC

t_S		f_{ADC}= 60 MHz	0.18	-	4.26	μs
			11	-	255	$1/f_{ADC}$
t_{CONV}	( )	f_{ADC}= 60 MHz 12	0.4	-	-	μs
		f_{ADC}= 60 MHz 10	0.37	-	-	μs
		f_{ADC}= 60 MHz 8	0.34	-	-	μs
		20 268 (Ts + n +1)				$1/f_{ADC}$
f_S	f_{ADC}= 60 MHz	12 ADC	-	-	2.5	Msps
t_{STT}		-	-	1	2	μs

3-5 2 ADC

1. 0 VAVCC VCREFH.2 V

5$,1

$$\frac{1}{d2}$$

1 1/4 LSB N = 1122

k ADC_SSTR

E_T			±4.5	±6	LSB
E_O		f_{ADC}=60MHz	±3.5		
		<10K			
		V_{REFH}=V_{AVCC}=2.4~3			

ENOB		f_{ADC}=30 MHz =2 kHz =0 ohm V_{REFH}=V_{AVC}=1.8 V	10.	-	Bit
SINAD			67.	-	dB
SNR			67.	-	dB
THD			-	-75.	dB

3-55 ADC123_IN0~32_IN4, ADC12_IN12_IN14, ADC3_IN16~19 @ f_{ADC}=80 / 30 MHz

E_T		f_{ADC}=60 MHz <1 kΩ V_{REFH}=V_{AVC}=2.4 ~ 3	±5.5	±7	LSB
E_O			±4.5	±7	LSB
E_G			±4.5	±7	LSB
E_D			±1.5	±3	LSB
E_L			±2.0	±4	LSB

3-55 ADC12_IN14, ADC3_IN4~15 @ f_{ADC}=60 MHz

E_T		f_{ADC}=80 / 30 MHz <1 kΩ V_{REFH}=V_{AVC}=1.8 V	±5.5	±7	LSB
E_O			±4.5	±7	LSB
E_G			±4.5	±7	LSB
E_D(1)			±1.5	±3	LSB
E_L(1)			±2.0	±4	LSB

3-56 ADC12_IN14, ADC3_IN4~15 @ f_{ADC}=30 MHz

1.

ENOB		f_{ADC}=60 MHz =2 kHz =0 ohm V_{REFH}=V_{AVC}=2.4 ~ 3.	10.	-	Bit
SINAD			64.	-	dB
SNR			64.	-	dB
THD			-	-80.	dB

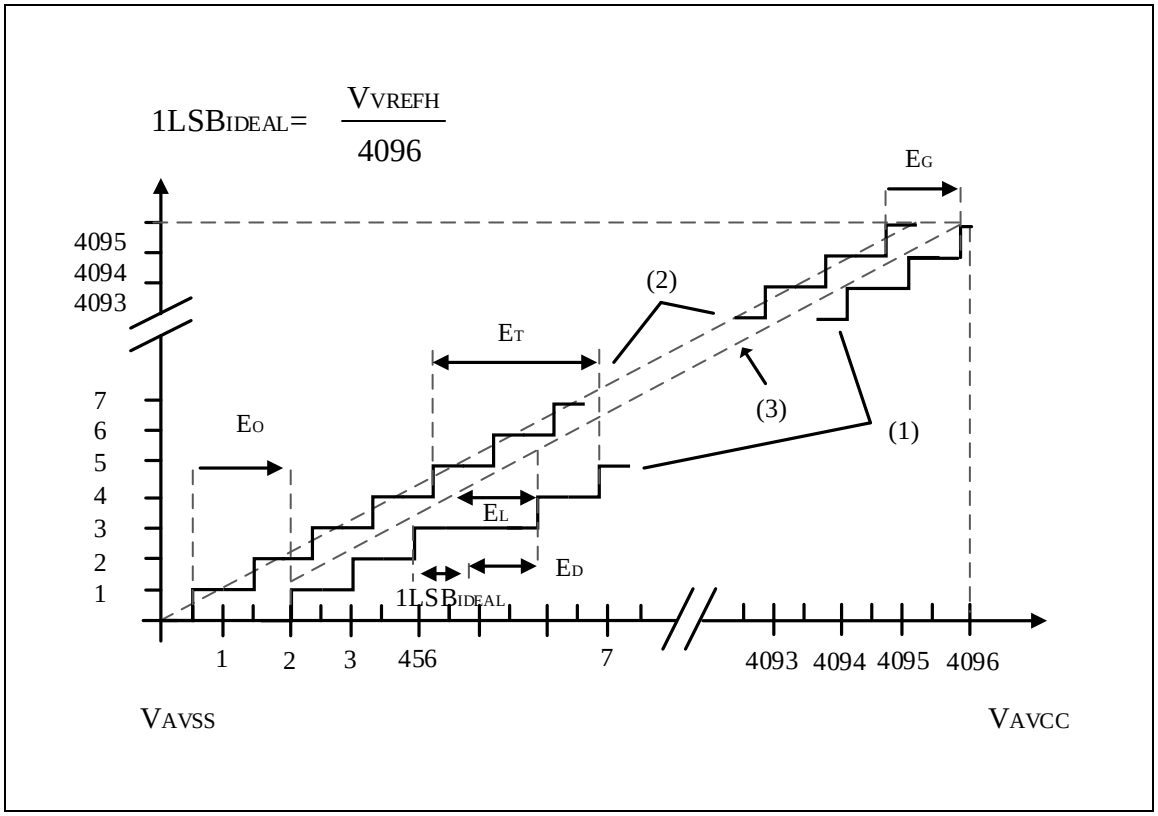
3-57 ADC12_IN1ADC12_IN4~15 @ f_{ADC}=60 MHz

ENOB		f_{ADC}=83.0 MHz =2 kHz =0 ohm V_{REFH}=V_{AVC}=1.8	10.	-	Bit
SINAD			66.	-	dB
SNR			66.	-	dB
THD			-	-79.	dB

3-58 ADC12_IN1ADC12_IN4~15 @ f_{ADC}=83.0 MHz

E_T		f_{ADC}=60 MHz =1 Kω V_{REFH}=V_{AVC}=2.7 ~ 3.6	±6.0	±8.0	LSB
E_O			±6.0	±8.0	LSB
E_G			±6.0	±8.0	LSB
E_D			±2	±3	LSB
E_L			±3	±4	LSB

3-9 ADC + @ f_{ADC}=60 MHz



3-3 1 A D C

1.

2.

3.

4.

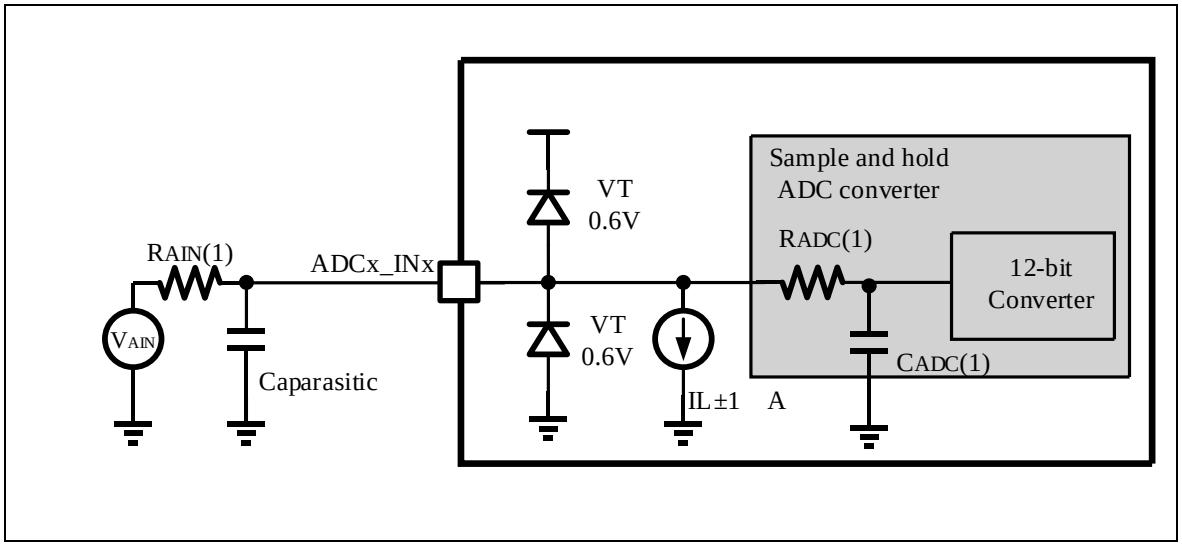
5. E_T =

   E_O =

   E_G =

   E_D =

   E_L =



3-3 2 A D C

1. RAI N RADC CADC 3-5 1

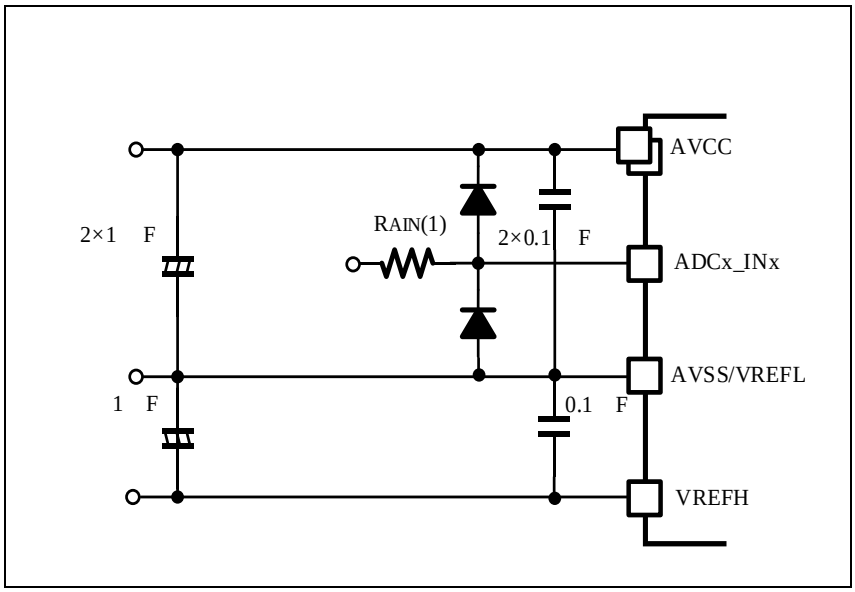
2. C p a r a s i t PCB P C B 5 PC p a r a s i t i c

Fa d c

3 & %

V R E F H A V C C A V C C

0 .µF



3-3 3

3.3.25

V_{AVCC}		-	1.8	3.3	3.6	V
Aref		= $_{A}V_{CC}$	1.8	3.3	3.6	V
AO		-	0	-	Aref 1 LSB	V
CL		-	-	-	20	Pf
RO		-	-	8.6	12	kΩ
DNL	-1 LSB	-	-	-	2	LSB
TUE		-	-	-	24	LSB
T_{st}	DAC ±4 LSB 12 CL=10Pf	-	-	0.9	1.2	μs
Iavcc		-	-	0.1	2	μA
Iaref		-	-	146	260	μA

3-5 7 12bit DAC

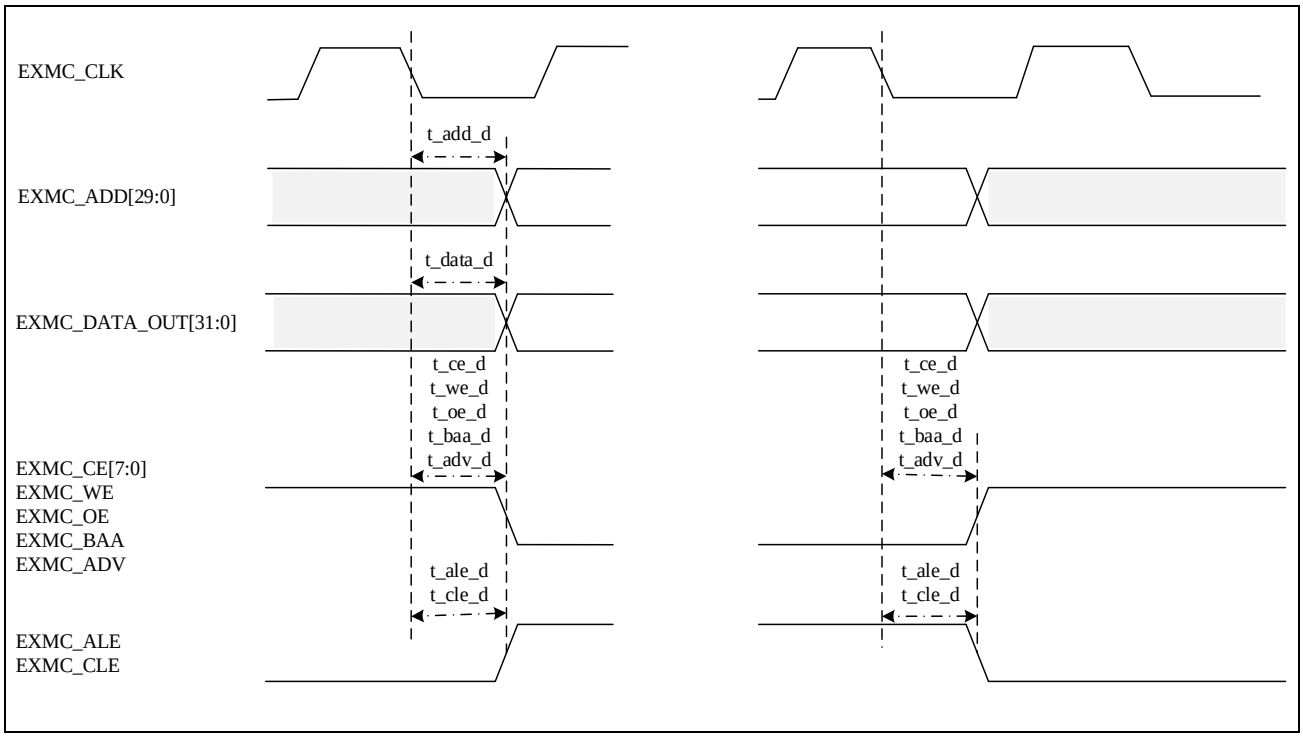
VAVCC		-	1．8	3．3	3．6	V
Aref		=AVCC	1．8	3．3	3．6	V
AO			0		Aref 1LSB	
DNL	-1LSB	-	-	-	2	LSB
TUE		-	-	-	5	LSB
Tst	DAC ±1 LSB 12 Vav≥c2c．7	-	-	65．	81	ns
	DAC ±32 LSB 12 Vav≥c2c．7	-	-	36	44．9	ns
	DAC ±1 LSB 12 Vavcc<2．7	-	-	-	83．8	ns
	DAC ±32 LSB 12 Vavcc<2．7	-	-	-	48．5	ns
Iavcc		-	-	0．1	2	μA
Iaref		-	-	146	260	μA

3-5 8 12bit DAC

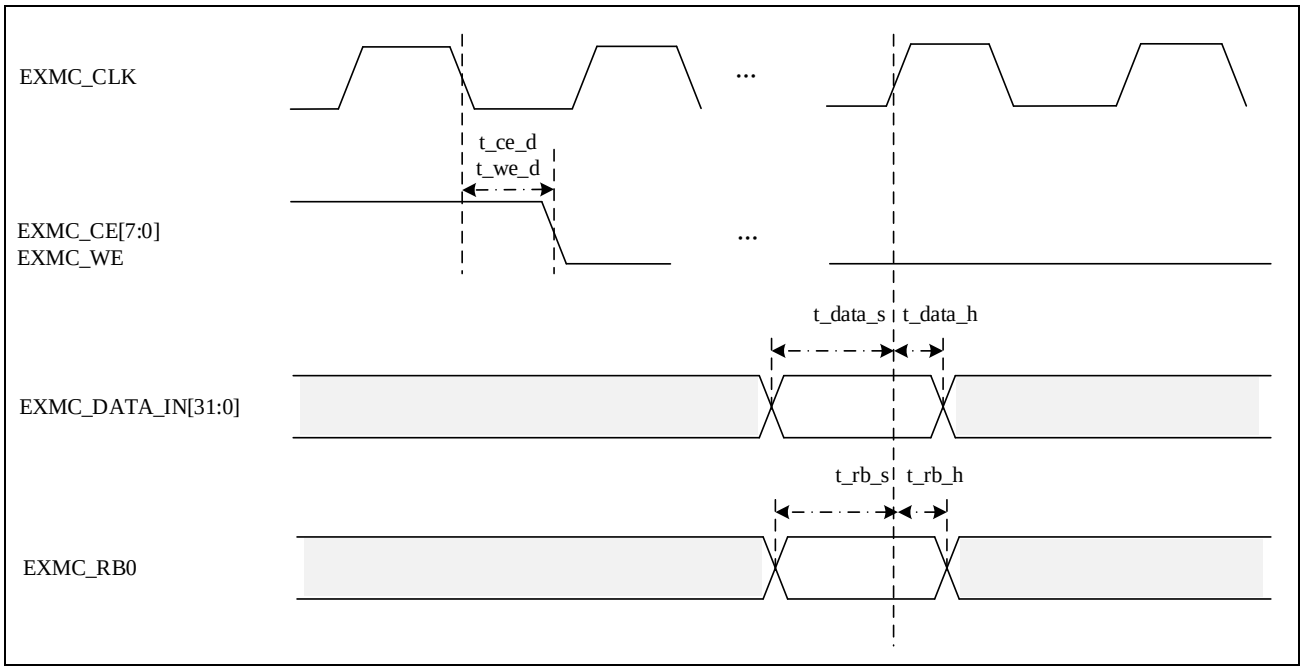
3.3.28 (; 0 &

6\PERO	3DUDPHWHU	0LQ	7\S	0D[	8QLV
t_add_d	2.7V~3.6V	-	-	12	ns
	1.8V~2.7V	-	-	18	ns
t_data_d	2.7V~3.6V	-	-	12	ns
	1.8V~2.7V	-	-	18	ns
t_ce_d	CE 2.7V~3.6V	-	-	9	ns
	CE 1.8V~2.7V	-	-	12	ns
t_we_d	WE 2.7V~3.6V	-	-	9	ns
	WE 1.8V~2.7V	-	-	12	ns
t_oe_d	OE 2.7V~3.6V	-	-	9	ns
	OE 1.8V~2.7V	-	-	12	ns
t_baa_d	BAA 2.7V~3.6V	-	-	9	ns
	BAA 1.8V~2.7V	-	-	12	ns
t_adv_d	ADV 2.7V~3.6V	-	-	9	ns
	ADV 1.8V~2.7V	-	-	12	ns
t_ale_d	ALE 2.7V~3.6V	-	-	9	ns
	ALE 1.8V~2.7V	-	-	12	ns
t_data_s	Setup 2.7V~3.6V	24	-	-	ns
	Setup 1.8V~2.7V	28	-	-	ns
t_data_h	Hold	0	-	-	ns
t_rb_s	RB Setup 2.7V~3.6V	24	-	-	ns
	RB Setup 1.8V~2.7V	28	-	-	ns
t_rb_h	RB Hold	0	-	-	ns

3-6 1 EXMC



3-3 4 EXMC



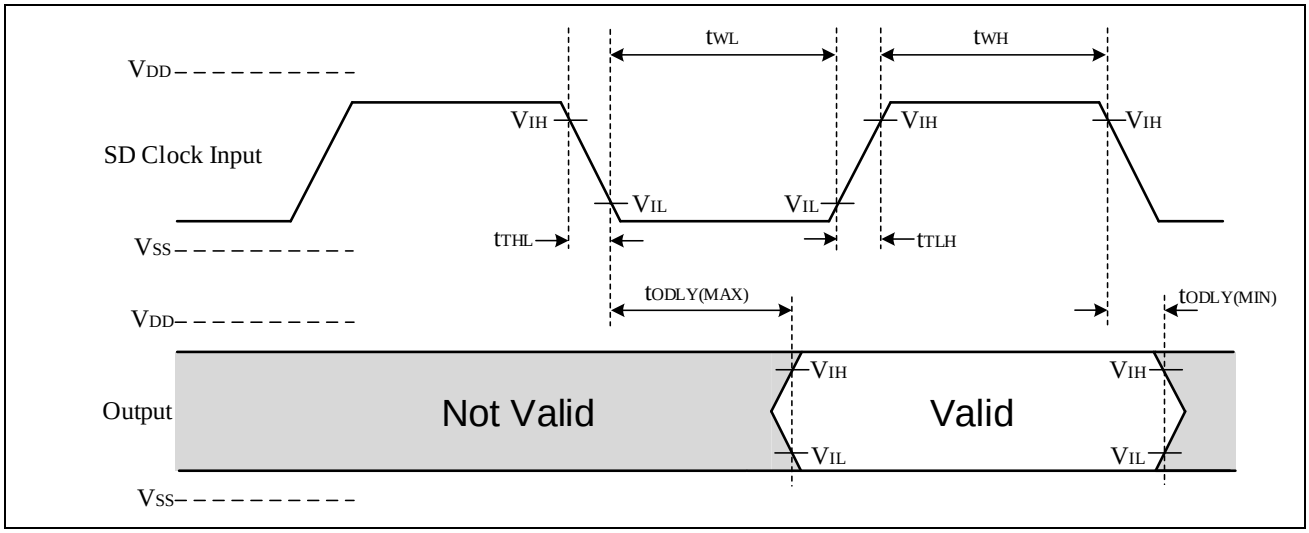
3-3 5 EXMC

3.3.29 '93

6\PER	3DUDPHWHU	0LQ	7\S	0D[	8QL
tpix_csl	DVPP_IXCSLKtup 2.7V~3.6V	6	-	-	ns
	DVPPIXCLK Setup 1.8V~2.7V	9	-	-	ns

tpix_chl

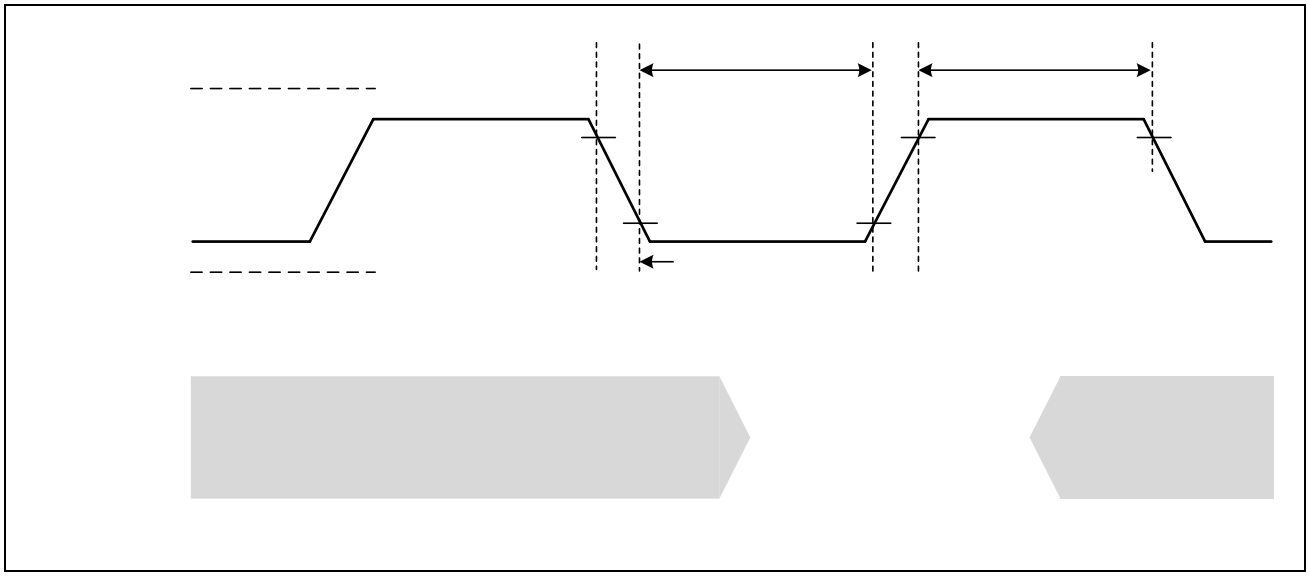
DVP VSYNC



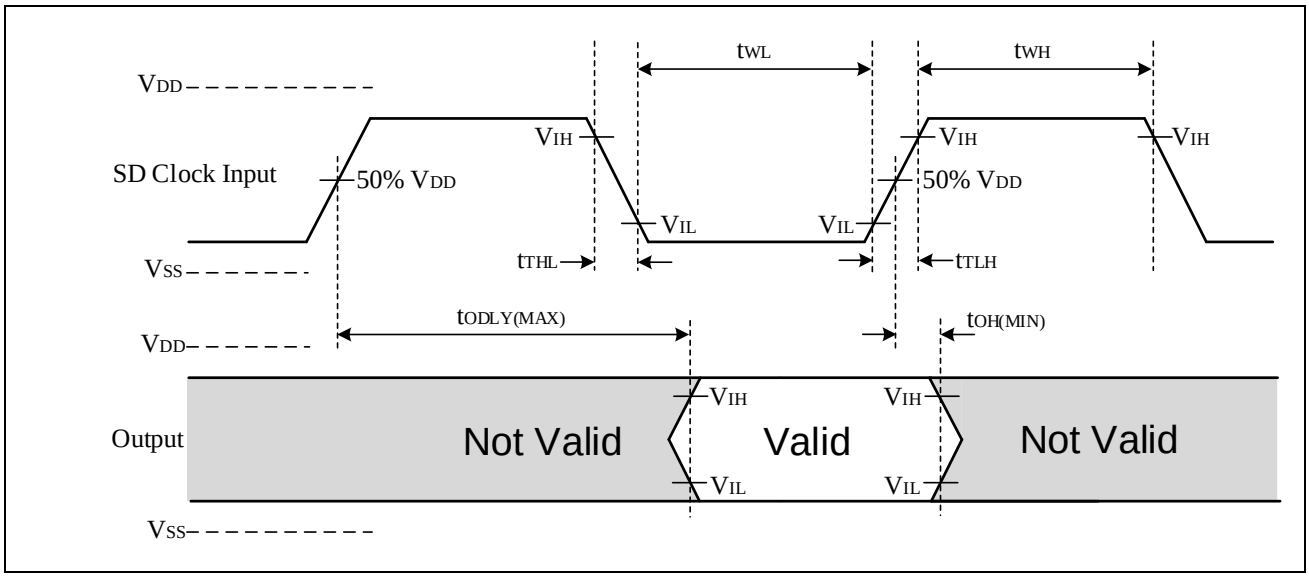
3-3 8

-		1.8	3.6	V	
f_{PP}		-	25	MHz	C = 30 Pf
f_{OD}		-	400	kHz	C = 30 Pf
t_{WL}		10	-	ns	C = 30 Pf
t_{WH}		10	-	ns	C = 30 Pf
t_{TLH}		-	10	ns	C = 30 Pf
t_{THL}		-	10	ns	C = 30 Pf
t_{ISU}		5	-	ns	C = 30 Pf
t_{IH}		14	-	ns	C = 30 Pf
t_{ODLY}		1	14	ns	C = 30 Pf

3-6 3



3-3 9


VDD
SD Clock Input
VSS
VDD
Output
VSS
tWL
tWH
VIH
VIL
50% VDD
tTHL
tTLH
tODLY(MAX)
tOH(MIN)
Not Valid
Valid
Not Valid

3-4 0

-		1.8	3.6	V	
f_{PP}		-	50	MHz	C = 30 P
f_{OD}		-	400	kHz	C = 30 P
t_{WL}		7	-	ns	C = 30 P
t_{WH}		7	-	ns	C = 30 P
t_{TLH}		-	3	ns	C = 30 P
t_{THL}		-	3	ns	C = 30 P
t_{ISU}		5	-	ns	C = 30 P
t_{IH}		14	-	ns	C = 30 P
t_{ODLY}		-	14	ns	C = 30 P
t_{OH}		3	-	ns	C = 30 P

3-64

3.3.31

V_{AVCC}			-	1.8	3.3	3.6	V
V_{OS}(1)			-	-8	-	8	Mv
V_I			-	0.1*AVCC Ga	-	0.9*AVCC Ga	V
G_E		PGAVSS PGA	Gain=1/2	-1	-	1	%
			Gain=2/3	-1	-	1	%
			Gain=2	-1	-	1	%
			Gain=2.5	-1	-	1	%
			Gain=3	-1	-	1	%
			Gain=3.5	-1.5	-	1.5	%
			Gain=4	-1.5	-	1.5	%
			Gain=4.5	-1.5	-	1.5	%
			Gain=5	-2	-	2	%
			Gain=6	-2	-	2	%
			Gain=6.5	-3.0	-	3.0	%
			Gain=8	-3.0	-	3.0	%
			Gain=10	-4.0	-	4.0	%
			Gain=16	-4.0	-	4.0	%
			Gain=32(1)	-7.0	-	7.0	%
		AVSS PGA	Gain=1/2	-2	-	2	%
			Gain=2/3	-2	-	2	%
			Gain=2	-2	-	2	%
			Gain=2.5	-2	-	2	%
			Gain=3	-2	-	2	%
			Gain=3.5	-2.5	-	2.5	%
			Gain=4	-2.5	-	2.5	%

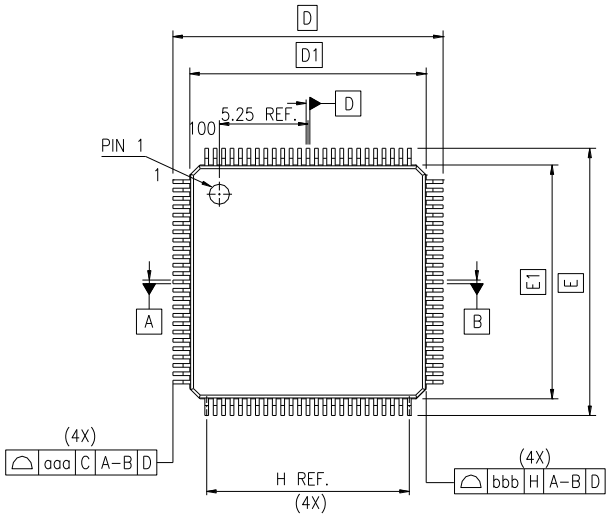
3.3.34 86$57 6723 5;

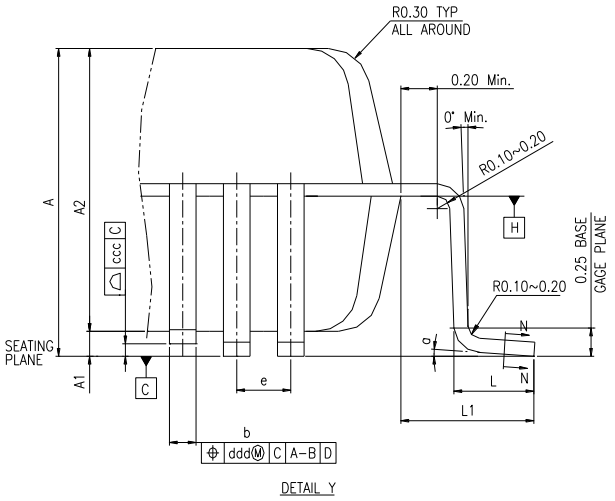
WF_USAR USART1 USART1_NFC.USAR0T 0.4 - 0.9 us

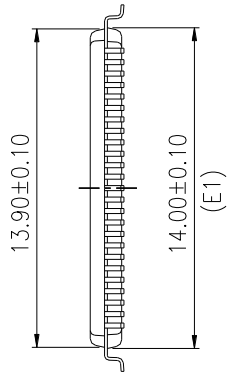
4

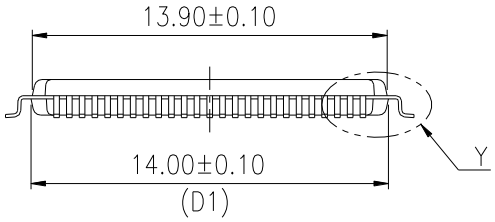
4.1

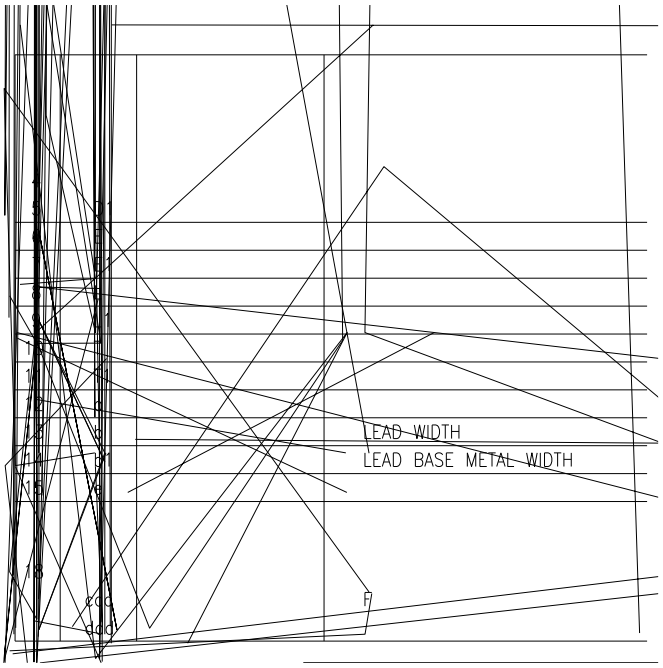
/4)3









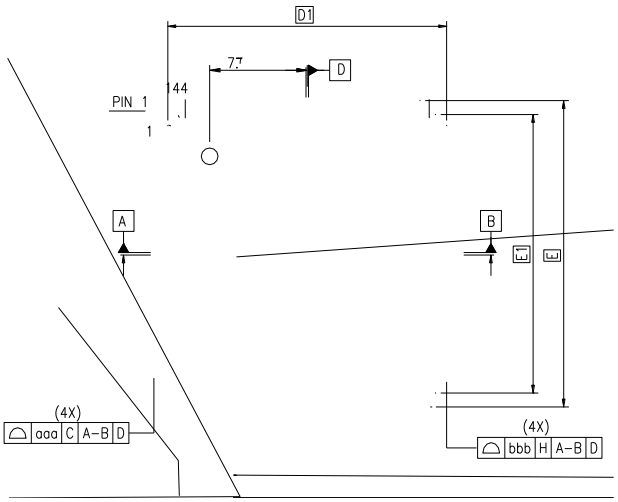


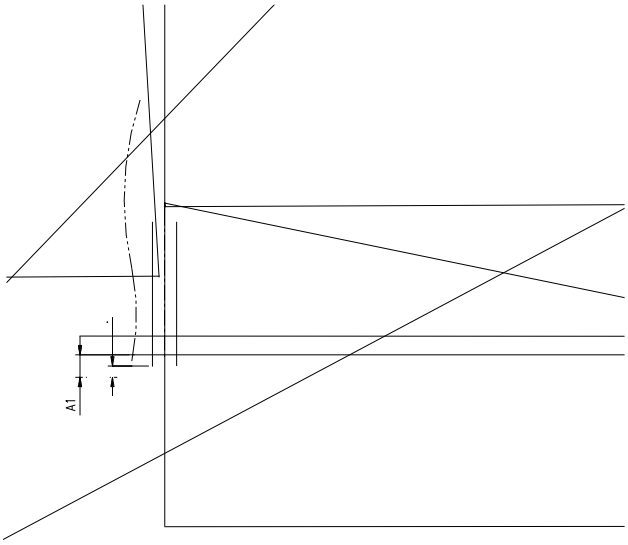
127(

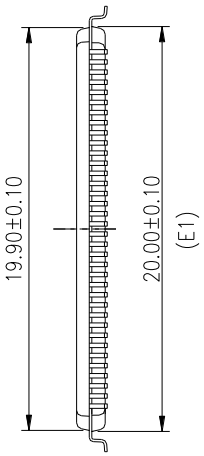
- 'LPHQVLRQVDQG(GR QRW LQFOX

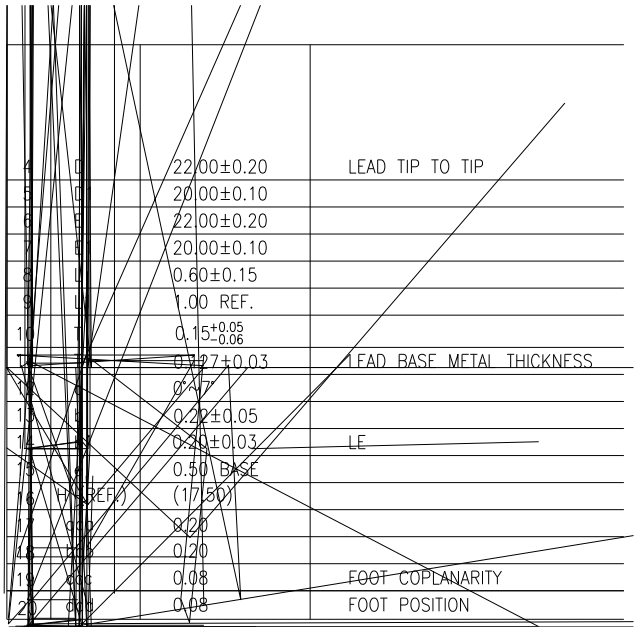
  PROG IODVK

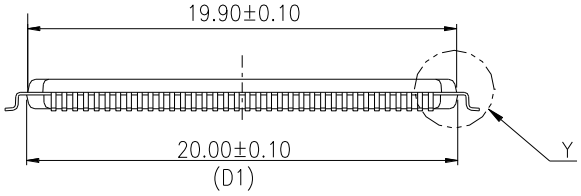
/4)3

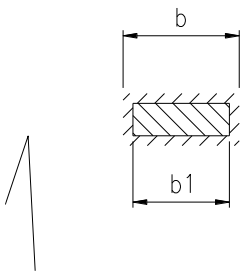








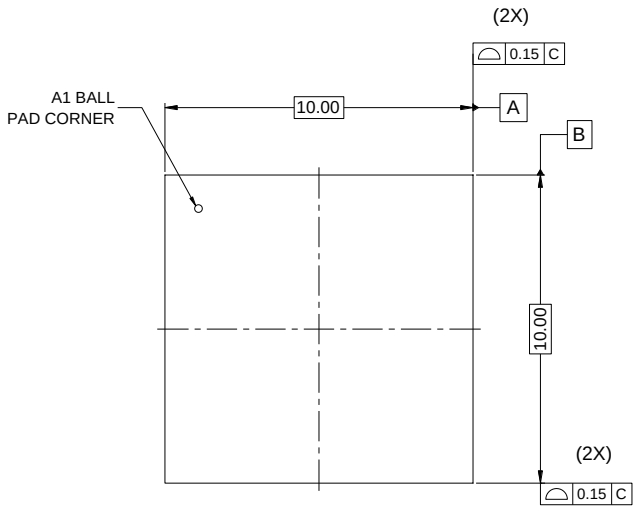




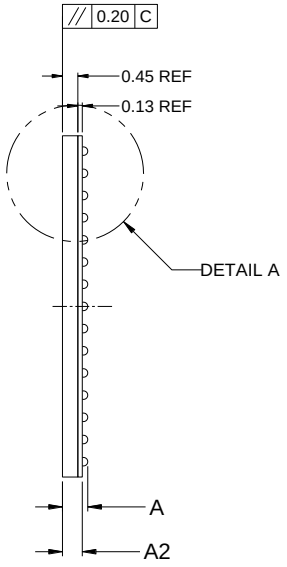
127(

- 'LPHQVLRQVDQG(GR QRW LQFOX PROG IODVK

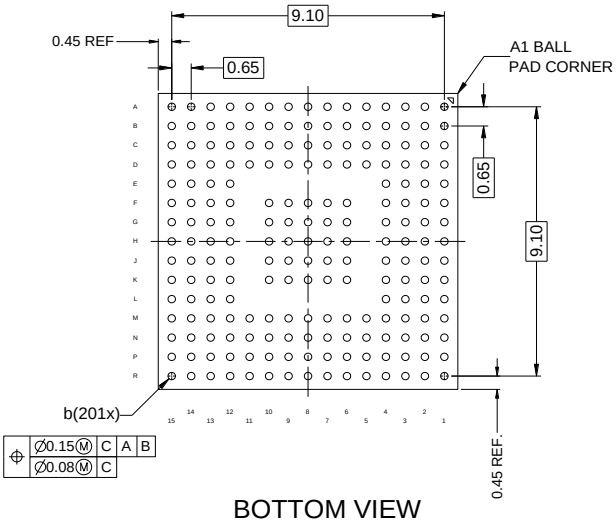
9) % * $



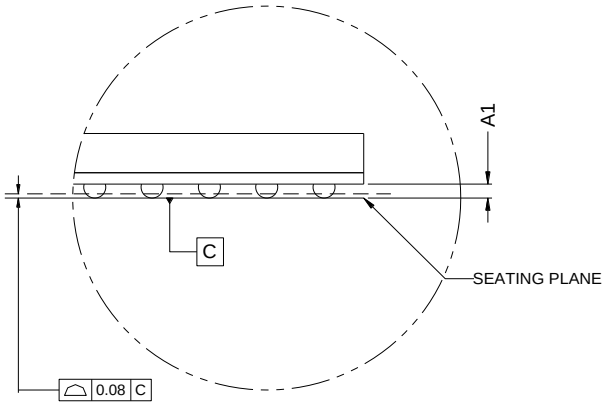
TOP VIEW



SIDE VIEW



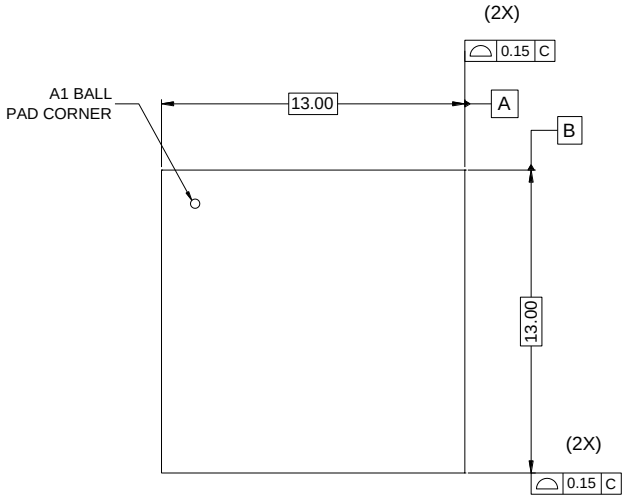
BOTTOM VIEW



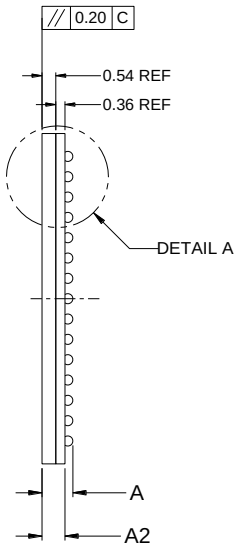
DETAIL A
ROTATED 90°

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	0.670	0.740	0.810
A1	0.110	0.160	0.210
A2	0.540	0.580	0.620
b	0.200	0.250	0.300
NUMBER OF BALL 201			

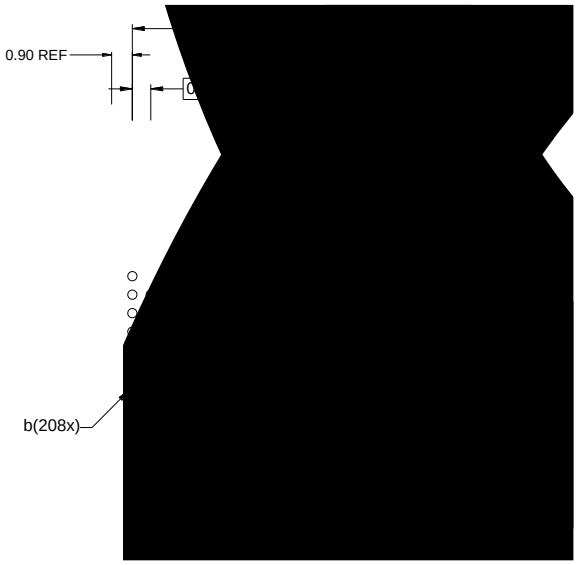
7) % * $

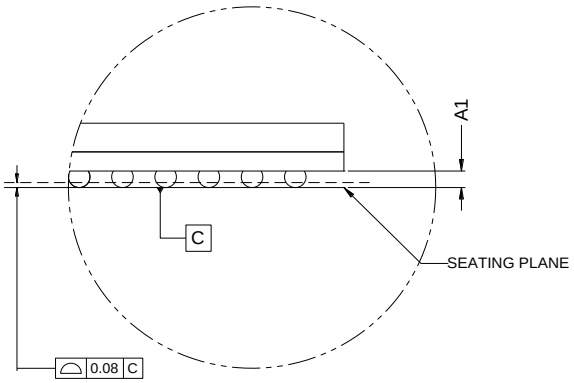


TOP VIEW



SIDE VIEW



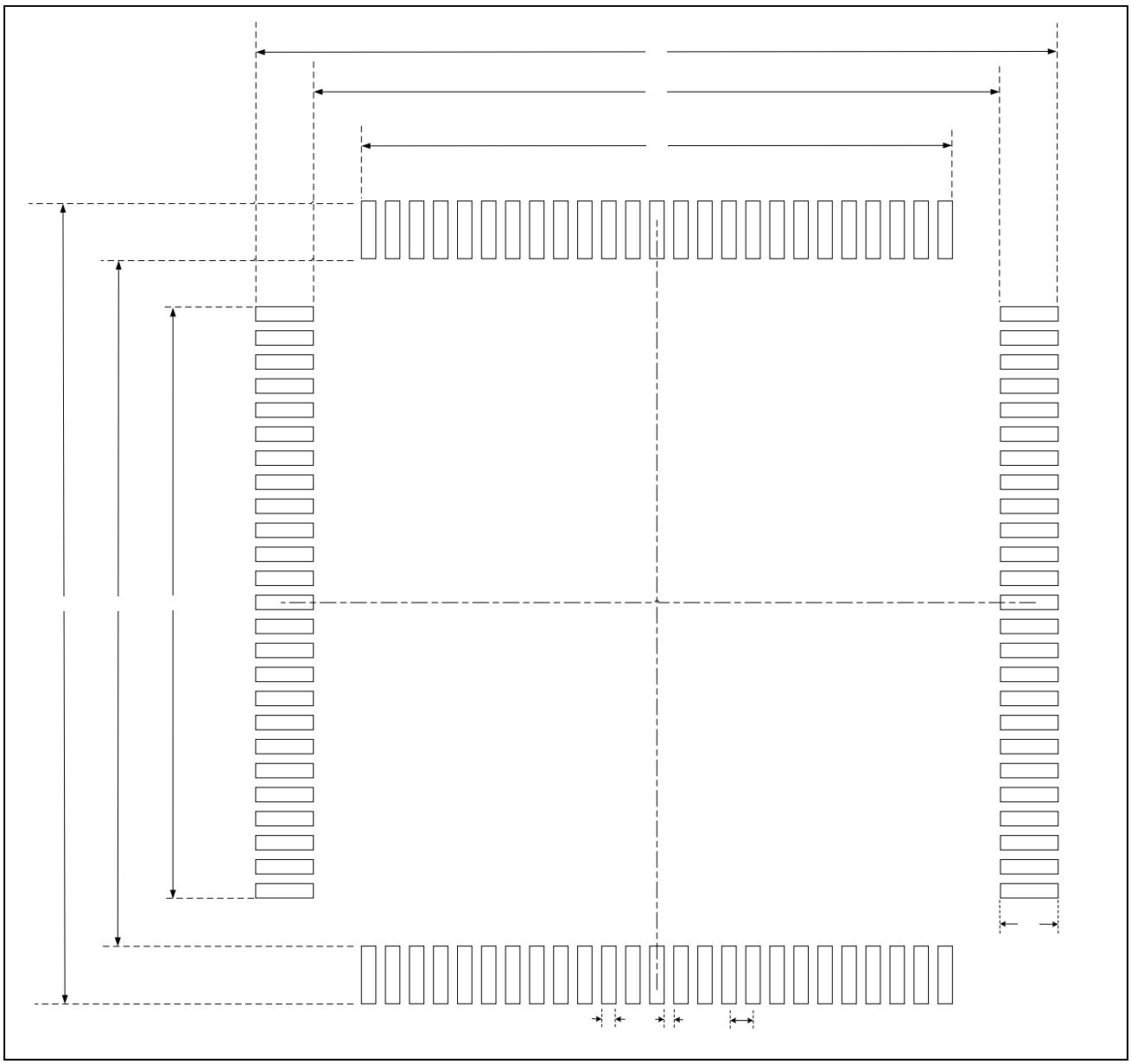


DETAIL A
ROTATED 90°

DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A	1.140	1.210	1.281
A1	0.260	0.310	0.360
A2	0.850	0.900	0.950
b	0.350	0.400	0.450
NUMBER OF BALL 208			

4.2

/4)3 PP [PP

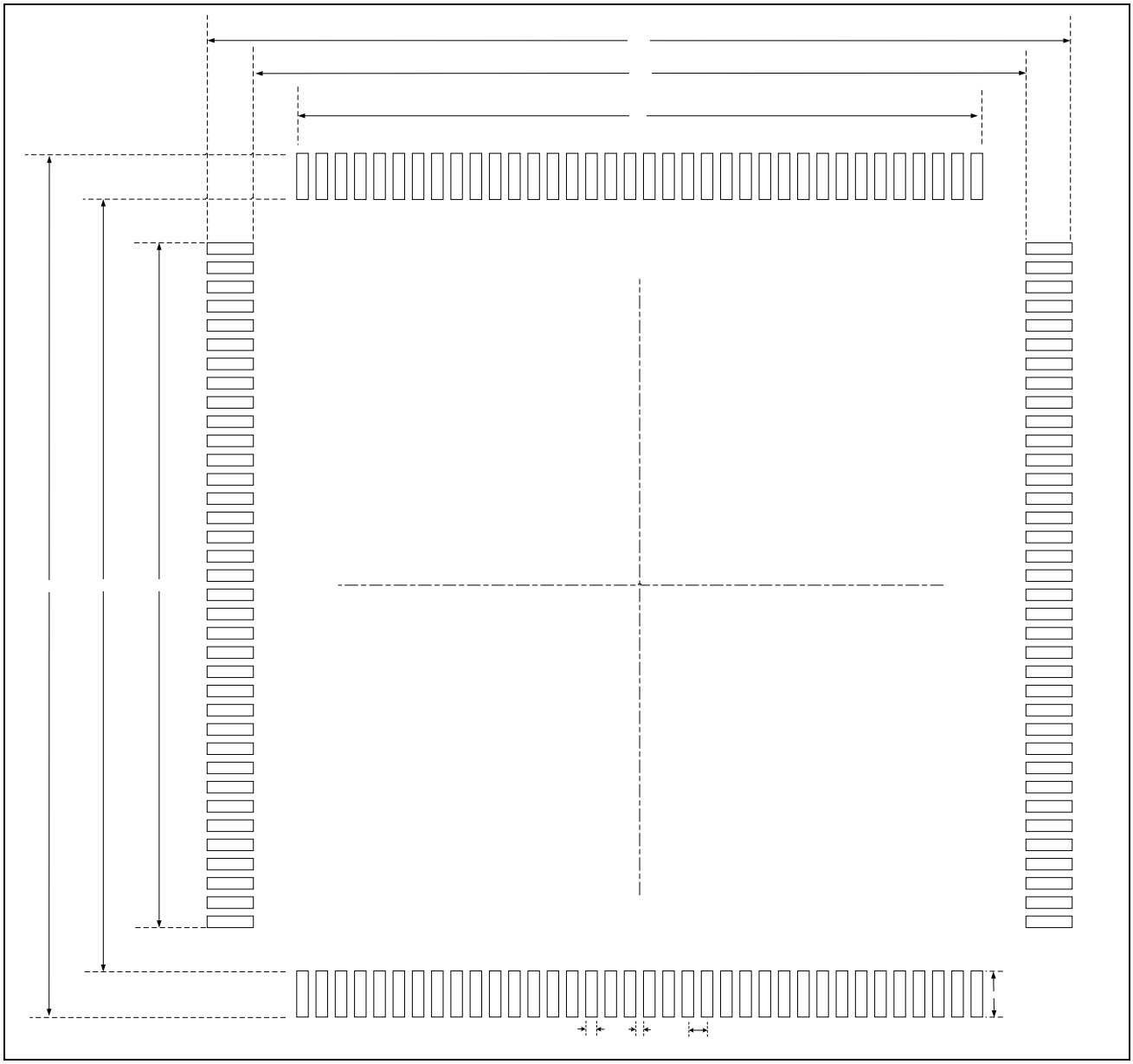


NOTE:

- Dimensions are expressed in millimeters.

-

/4)3 PP [PP

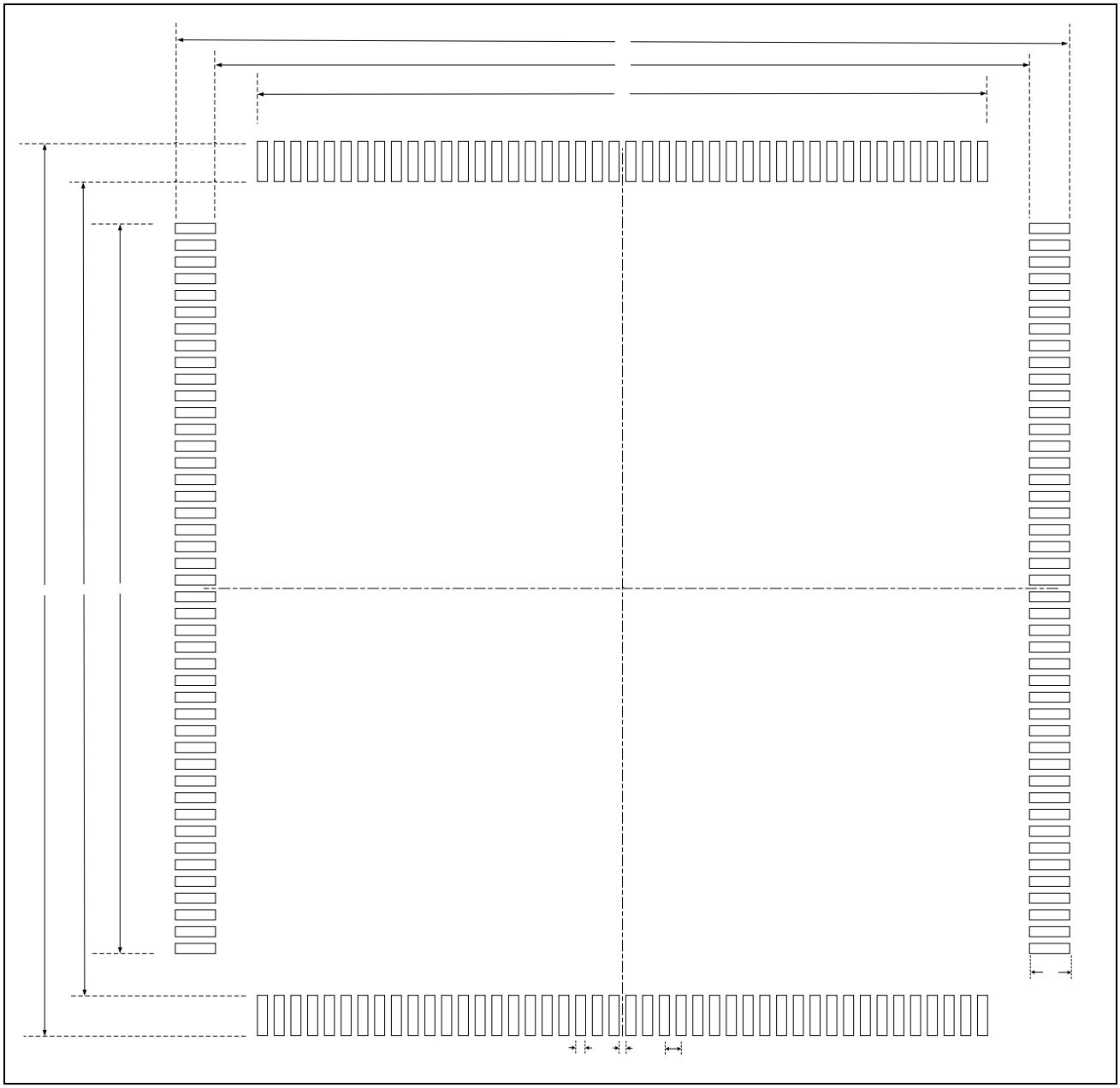


NOTE:

- Dimensions are expressed in millimeters.

-

/4)3 PP [PP

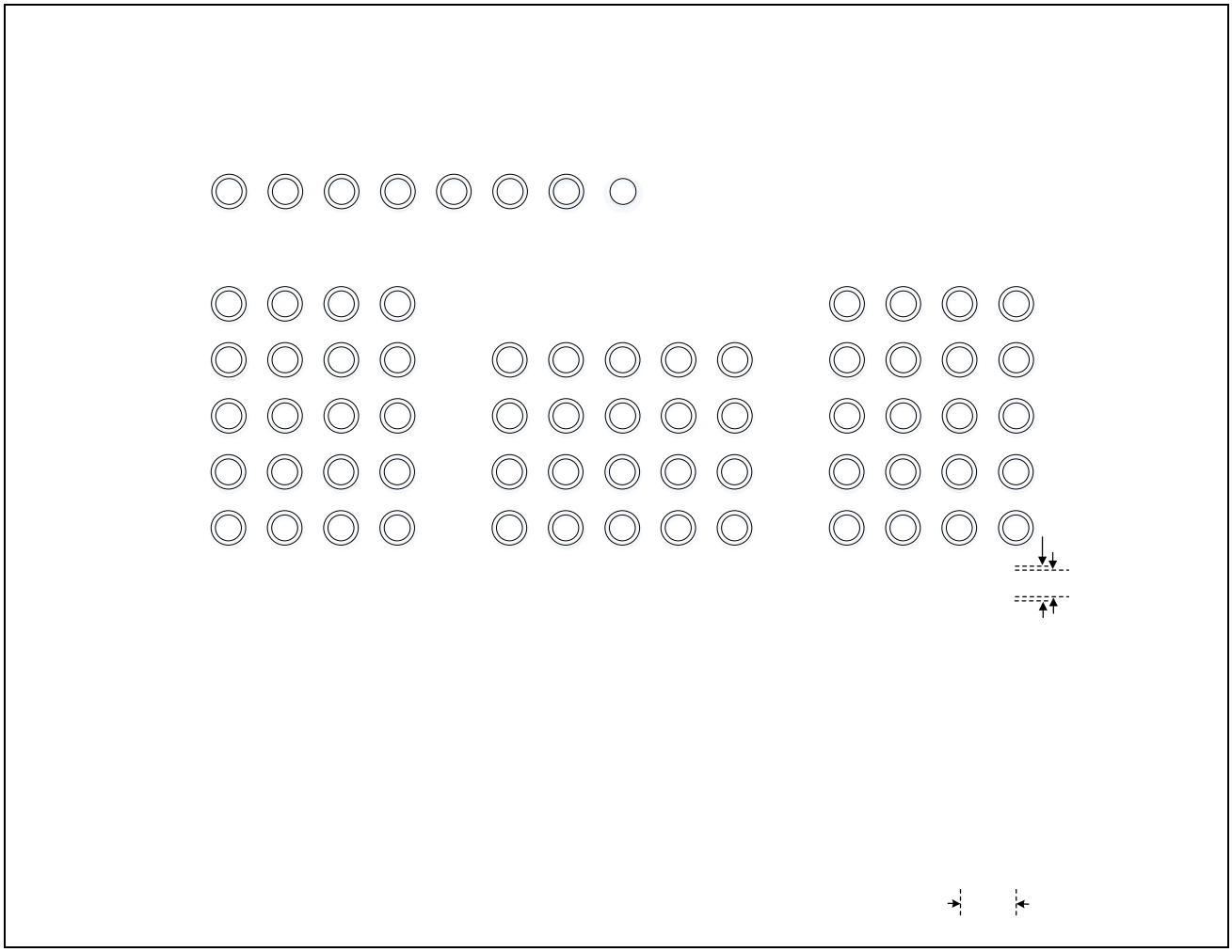


NOTE:

- Dimensions are expressed in millimeters.

-

9)%*$ PP [PP



NOTE:

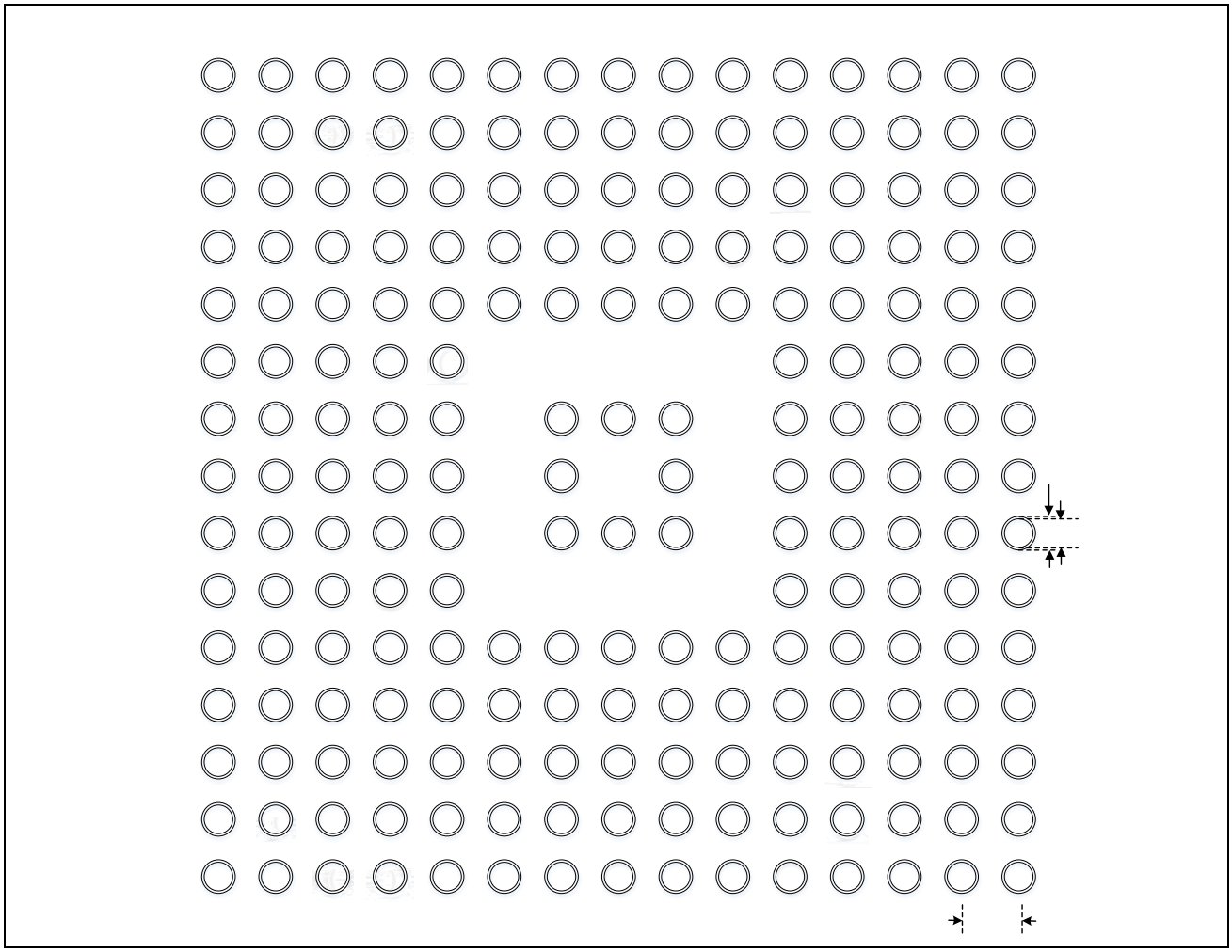
- Dimensions are expressed in millimeters.

-

VFBGA176recommended PCB design rules(0.65mm pitch

Dimension	Recommended values
Pitch	0.65mm
Dpad	0.280mm
Dsm	0.370mm typ. (depending on the solder mask registration)
Stencil opening	0.280mm
Stencil thickness	0.100mm

7)%*$ PP [PP



NOTE:

- Dimensions are expressed in millimeters.

-

TFBGA208 recommended PCB design rules (0.8mm pitch BC

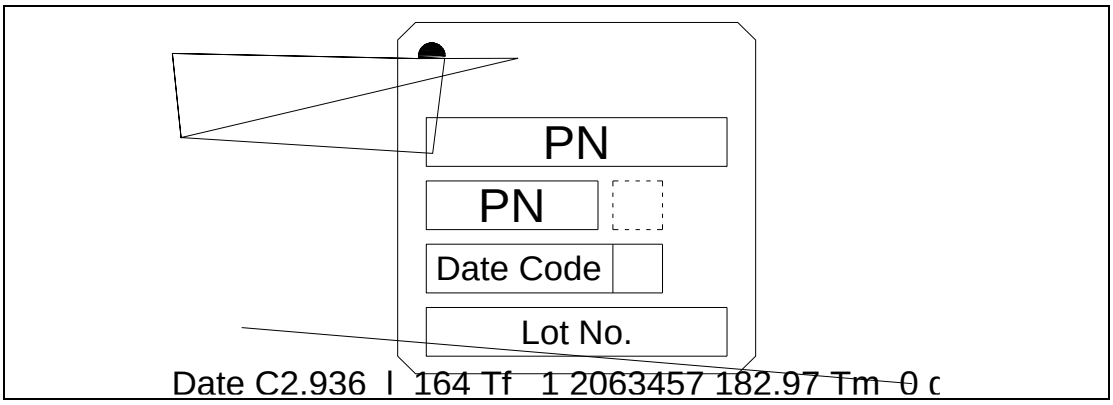
Dimension	Recommended values
Pitch	0.8mm
Dpad	0.400mm
Dsm	0.480mm typ. (depends on the solder mask regis
Stencil opening	0.400mm
Stencil thickness	Between 0.100mm and 0.125mm
Pad trace width	0.120mm

4.3

P i 1n

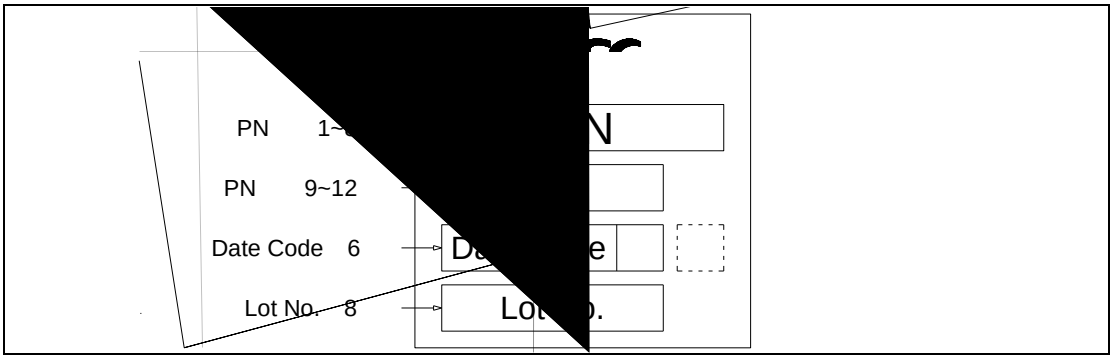
/ 4) 3 P Px P P / 4) 3 P P [P P

/ 4) 3 P P [P P



Date C2.936 l 164 Tf 1 2063457 182.97 Tm 0 c

9) % * $ P P [P P 7) % * $ P P [P P



-

4.4

T_j( )

$$T_J = {}_{a\ mb}T + {}_{D}(x\ \theta_{J\ A})$$

$T_{a\ mb}$

$\theta_{J\ A}$ /W

P_D I / O W

$I_{D\ DX}$ $_{DV}$ I / O I / O

5

&

Rev1.1	2021/01/11	
Rev1.0	2019/06/30	SRAM 512+4KB PWR_PWC_AOS 3-7 PLL/XTAL SMI CAN FD/CAN2.0B TBD 4~25MHz
Rev0.9	2018/03/09	Logo
Rev0.8	2018/04/08	3.3.13-32 CMOS 3.3.11 Schmit VIHL 3-6 3-7 3.3.23-46 UART “PCLK”1/6 “PCLK1”/32
Rev0.7	2022/05	1.4.6 1.4.7

Email:mcu@xhsc.com.cn

http://www.xhsc.com.cn

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